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MS-7399

Version 1.0

CPU:

Intel Prescott (L2=2MB)
 Intel Cendar Mill (65nm)
 Intel Smithfield (90nm Dual core)
 Intel Presler (65nm Dual core)
 Intel Conroe (65nm Dual core)
 Intel Kentsfield
 Intel Yorkfield
 Intel Wolfdale

System Chipset:

nVidia - MCP73PV/S

On Board Chipset:

BIOS -- SPI FLASH 4Mb
 Azalia CODEC(ALC 888S)
 LPC Super I/O -- ITE8718F
 LAN-Realtek RTL8211BL
 IEEE1394 -- VIA VT6308P

Main Memory:

DDR II * 2 (Max 2GB)

Expansion Slots:

PCI Express X16 SLOT * 1
 PCI Express X1 SLOT * 1
 PCI 2.3 SLOT * 2

Intersil PWM:

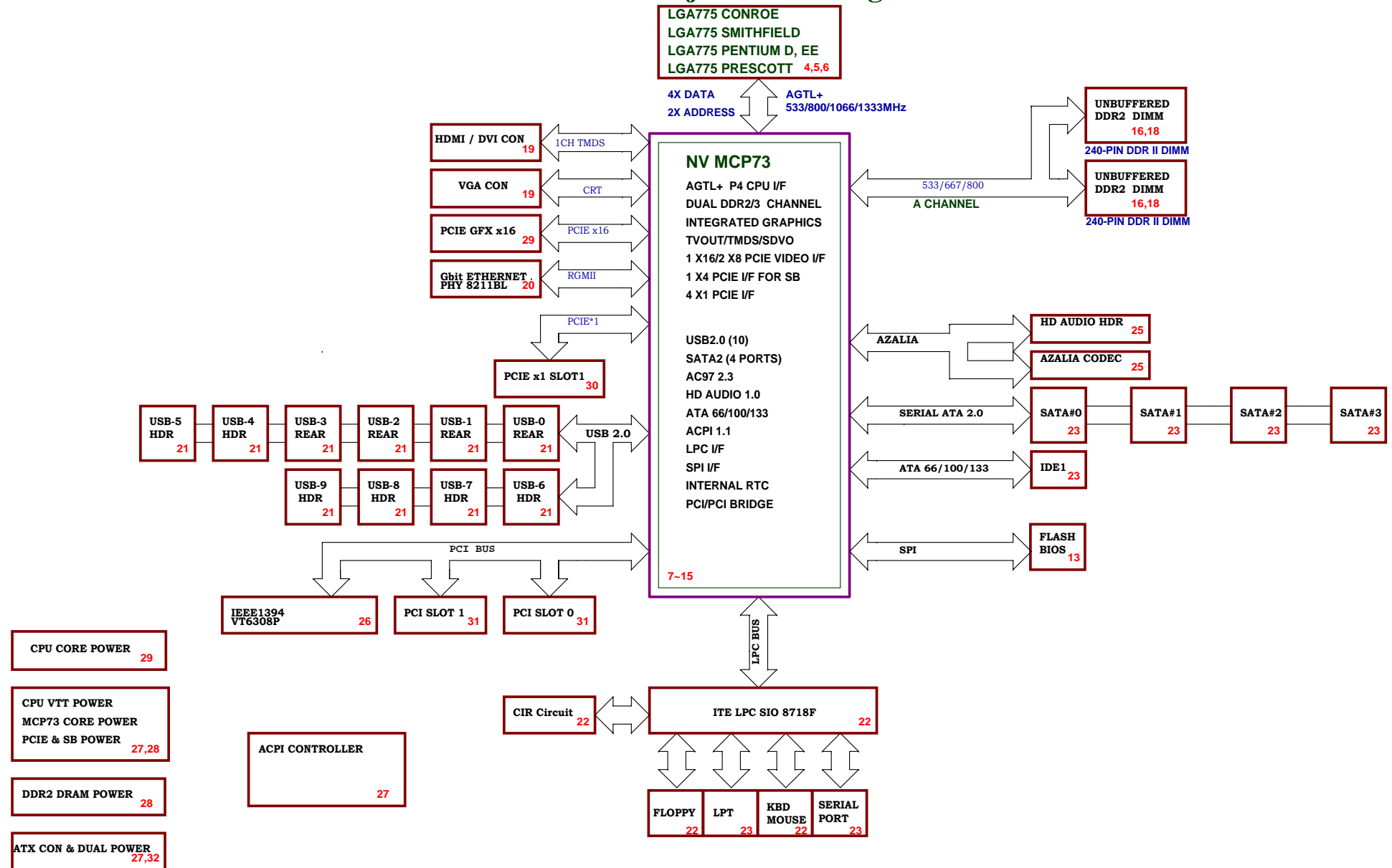
Controller: Intersil 6312 3 Phase



Persian Project

Veriton M463/M263
 DVI

acer Persian Project Block Diagram



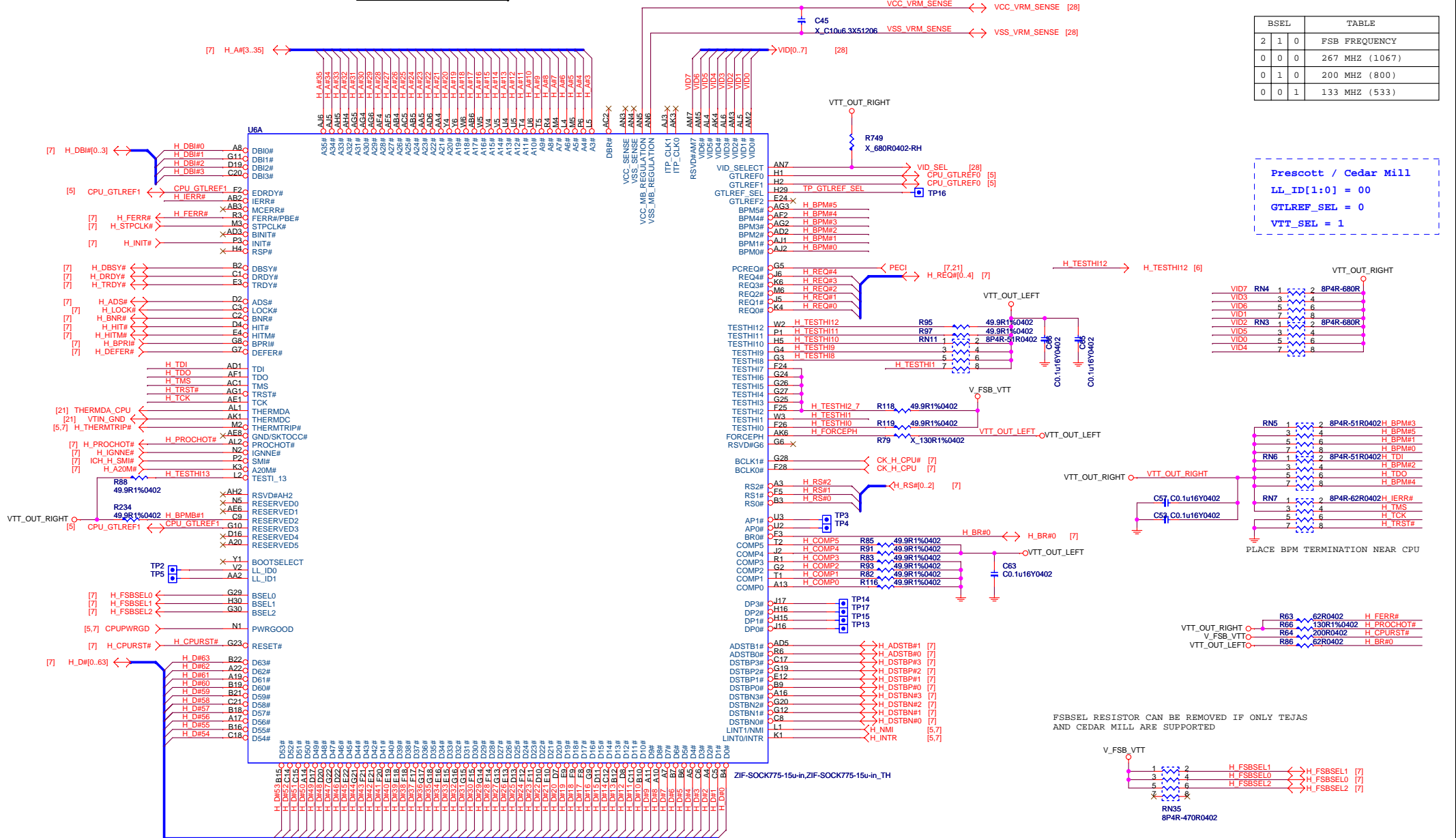
MCP73 GPIO Config.

GPIO Pin	Type	Primary State
GPIO_2/NMI/PS2_CLK0	I/O(S5_3.3V)	TMDS_DET1
GPIO_3/SMI#/PS2_DATA0	I/O(S5_3.3V)	TMDS_DET2
GPIO_4/SCI/INTR/PS2_CLK1	I/O(S5_3.3V)	Unused
GPIO_5/INIT#/PS2_DATA1	I/O(S5_3.3V)	OBR1
GPIO_6/FERR#/SYS_SERR#/IGPU_GPIO6	I/O(S5_3.3V)	Unused
GPIO_7/NFERR#/SYS_PERR#/IGPU_GPIO7	I/O(S5_3.3V)	Unused
GPIO_8/SPI_DI	I/O(S5_3.3V)	Unused
GPIO_9/SPI_DO	I/O(S5_3.3V)	Unused
GPIO_10/SPI_CS0	I/O(S5_3.3V)	Unused
GPIO_11/SPI_CLK	I/O(S5_3.3V)	Unused
LPC_DRQ1#/GPIO_19/FANRPM1	I/O(3.3V)	Unused
PROCHOT#/GPIO_20	I/O(CPU_VTT)	H_PROCHOT#
PE_WAKE#/GPIO_21	I/O(S5_3.3V)	WAKE#
HDA_SDATA_IN0/GPIO_22	I/O(S5_3.3V)	HDA_SDATA_IN
HDA_SDATA_IN1/GPIO_23/MGPIO_0	I/O(S5_3.3V)	Unused
HDA_SDATA_IN2/GPIO_24/MGPIO_2	I/O(3.3V)	Unused
USB_OC0#/GPIO_25	I/O(S5_3.3V)	OC#1
USB_OC1#/GPIO_26	I/O(S5_3.3V)	OC#2
USB_OC2#/GPIO_27	I/O(S5_3.3V)	OC#3
USB_OC3#/GPIO_28	I/O(S5_3.3V)	Pull Hi
USB_OC4#/GPIO_29	I/O(S5_3.3V)	Pull Hi
PCI_PME#/GPIO_30	I/O(S5_3.3V)	PCI_PME#
SIO_PME#/GPIO_31	I/O(S5_3.3V)	SIO_PME#
EXT_SMI#/GPIO_32	I/O(S5_3.3V)	LPC_SMI#
SUS_CLK/GPIO_34	I/O(S5_3.3V)	Unused
MII0_INTR/GPIO_35	I/O(S5_3.3V)	RGMI0_INTR#
MII0_PXER/GPIO_36/PWR_LED#	I/O(S5_3.3V)	RGMI0_RX_ER
MII0_PWRDWN/GPIO_37	I/O(S5_3.3V)	RGMI0_PREDN
PCI_REQ3#/GPIO_38/RS232_CTS#	I/O(3.3V)	PREQ#3
PCI_GNT3#/GPIO_39/RS232_RTS#	I/O(3.3V)	Unused
PCI_REQ2#/GPIO_40/RS232_DSR#	I/O(3.3V)	PREQ#2
PCI_GNT2#/GPIO_41/RS232_DTR#	I/O(3.3V)	PGNT#2
LPC_RESET#/GPIO_42	I/O(3.3V)	Unused
PCI_PERR#/GPIO_43/RS232_DCD#	I/O(3.3V)	PERR#
HDA_SYNC/GPIO_44	I/O(3.3V)	AZ_SYNC_R
HDA_SDATA_OUT/GPIO_45	I/O(3.3V)	HDA_SDATA_OUT
LPC_DRQ0#/GPIO_50	I/O(3.3V)	LPC_DRQ#0
PCI_REQ4#/GPIO52/RS232_SIN#	I/O(3.3V)	PREQ#4
PCI_GNT4#/GPIO_53/RS232_SOUT#	I/O(3.3V)	Unused
A20GATE/GPIO_55	I/O(3.3V)	A20GATE
KBRDRSTIN#/GPIO_56	I/O(3.3V)	KBRST#
SATA_LED#/GPIO_57	A(3.3V)	SATALED#
THERMTRIP#/GPIO_58	I/O(CPU_VTT)	H_THERMTRIP#
THERM#/GPIO_59	I/O(3.3V)	Unused
FANRPM0/GPIO_60	I/O(3.3V)	OBR2
FANCTL0/GPIO_61	I/O(3.3V)	AUDIO_FRONT_IO
FANCTL1/GPIO_62	I/O(3.3V)	DEPOP_GPIO
CABLE_DET_P/GPIO_63	I/O(3.3V)	ATADETO

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INTX# PCI_INTY# PCI_INTZ# PCI_INTW#	PREQ#0 PGNT#0	AD21	PCICLK0
PCI Slot 2	PCI_INTY# PCI_INTZ# PCI_INTW# PCI_INTX#	PREQ#1 PGNT#1	AD22	PCICLK1
1394	PCI_INTW#	PREQ#2 PGNT#2	AD23	1394_PCLK

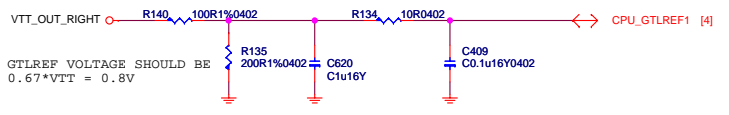
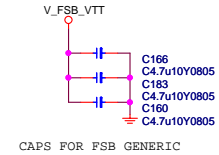
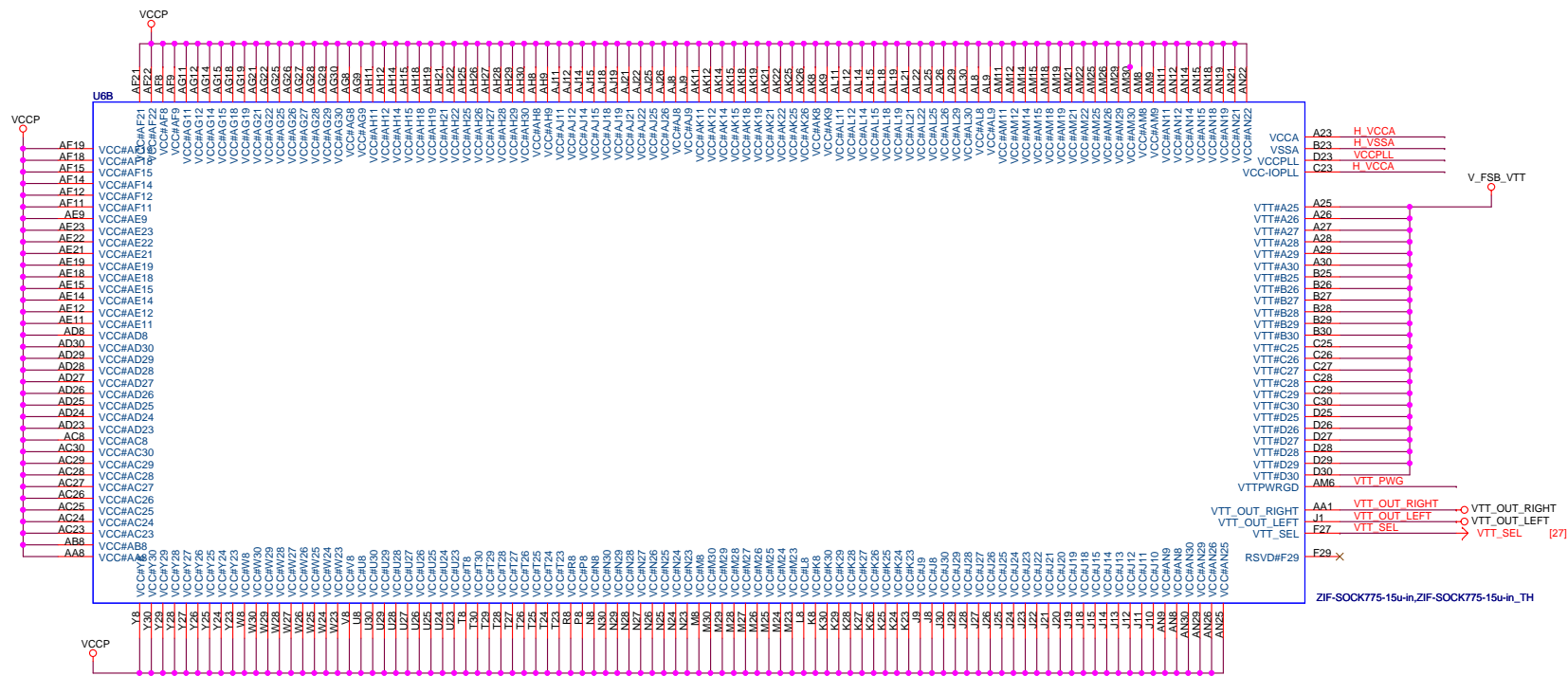
CPU SIGNAL BLOCK



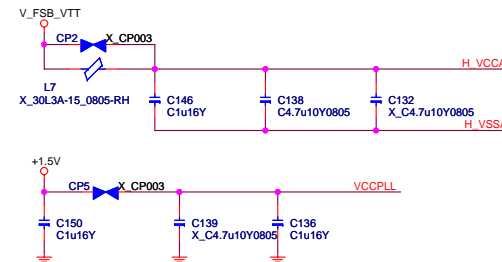
BSEL	TABLE
2 1 0	FSB FREQUENCY
0 0 0	267 MHZ (1067)
0 1 0	200 MHZ (800)
0 0 1	133 MHZ (533)

Prescott / Cedar Mill
 LL_ID[1:0] = 00
 GTLREF_SEL = 0
 VTT_SEL = 1

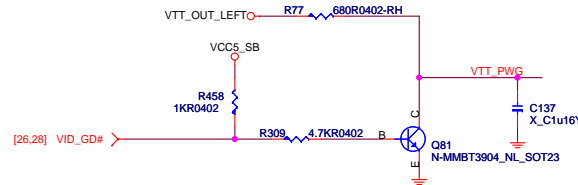
FSBSEL RESISTOR CAN BE REMOVED IF ONLY TEJAS AND CEDAR MILL ARE SUPPORTED

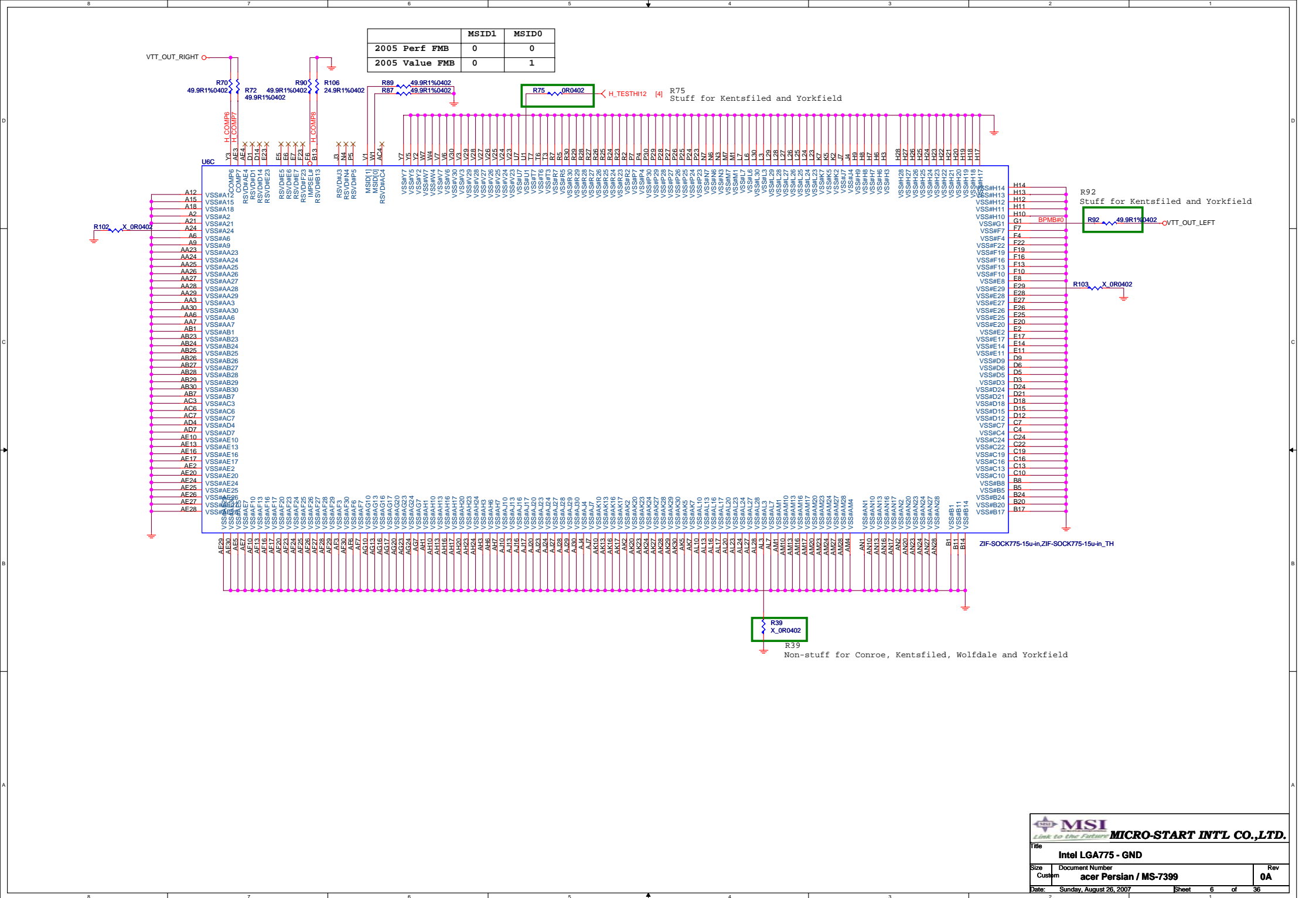


PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
TRACE WIDTH TO CAPS MUST BE SMALLER THAN 12MILS

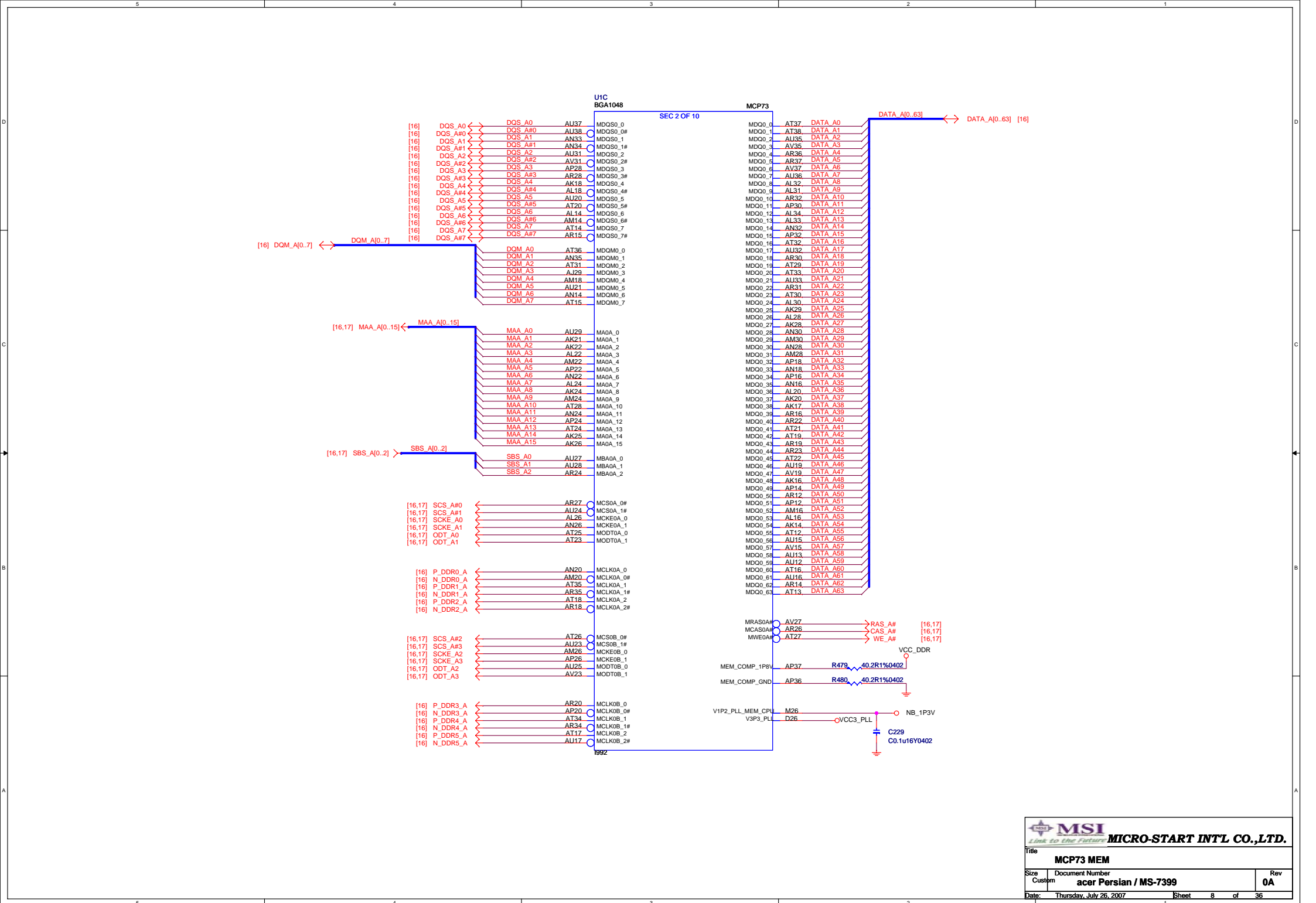


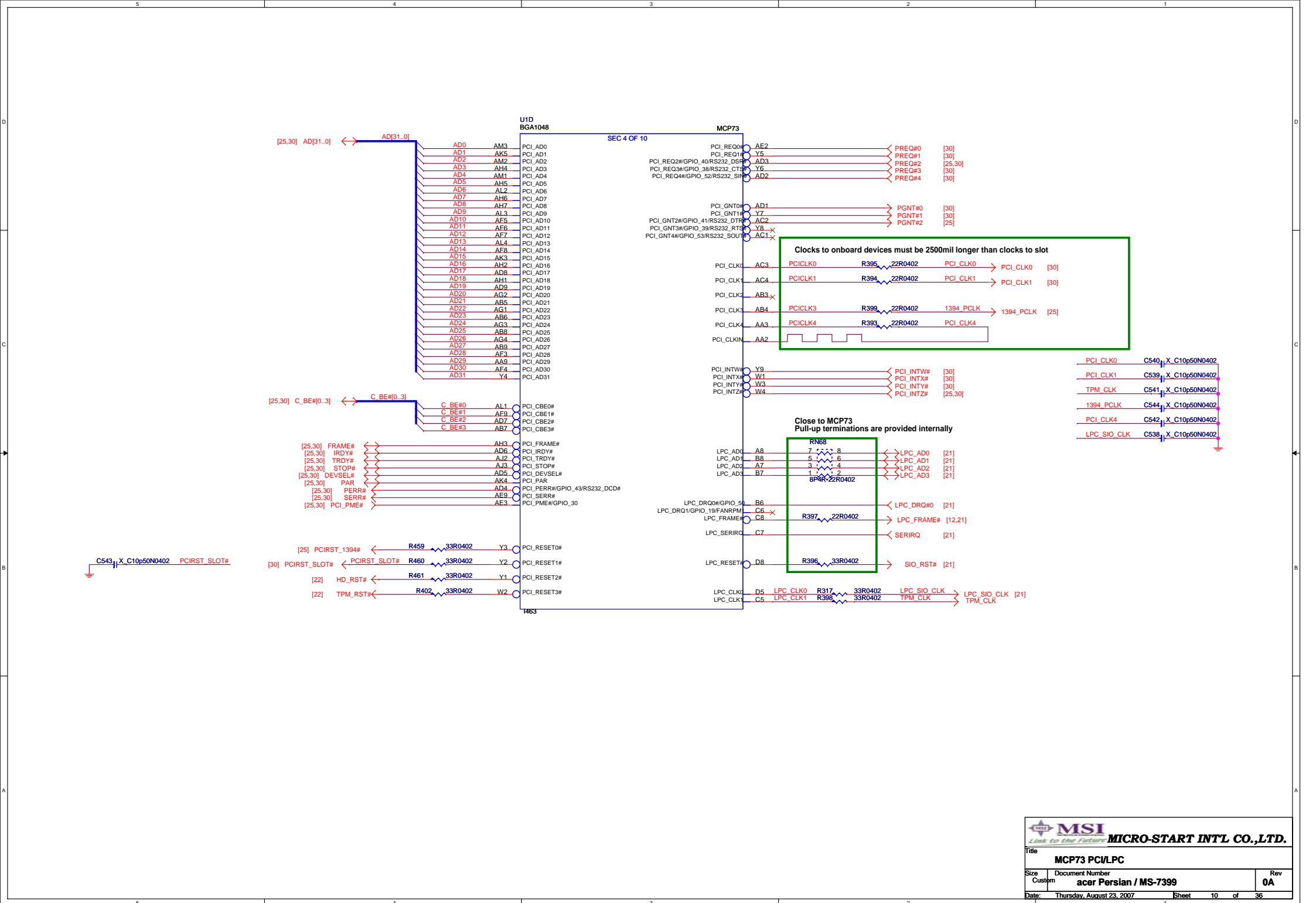
VTT_PWRGOOD

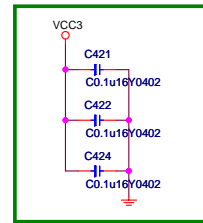
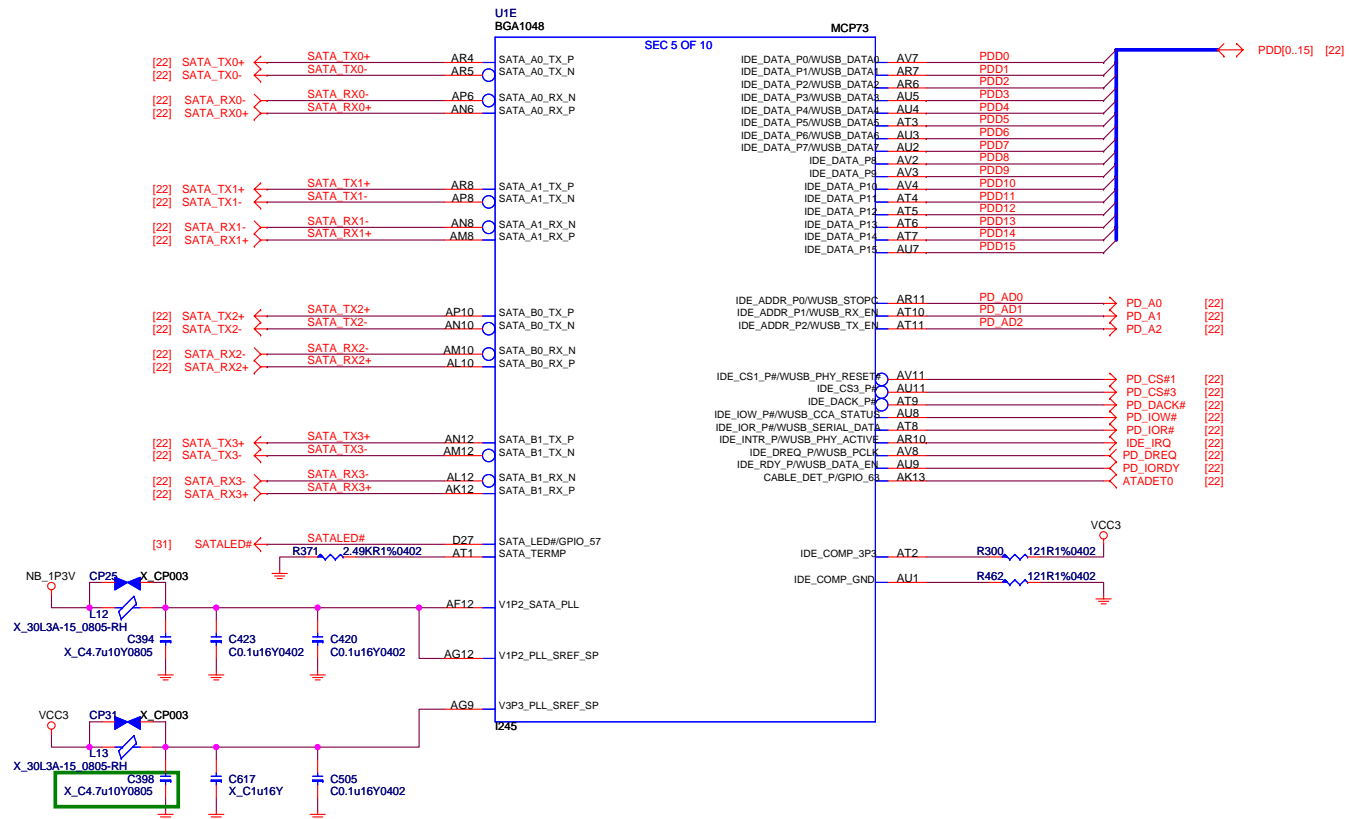




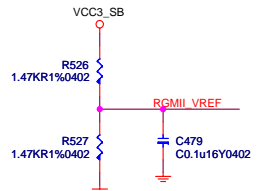
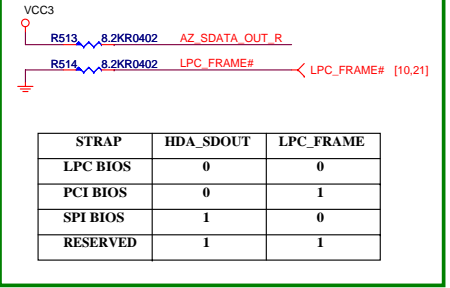
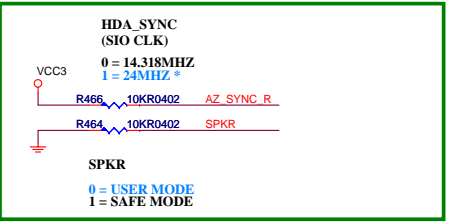
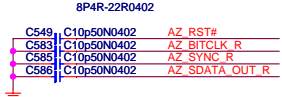
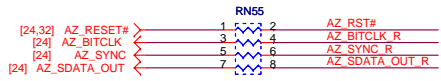
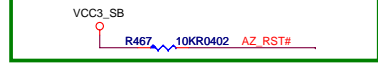
	MSID1	MSID0
2005 Perf FMB	0	0
2005 Value FMB	0	1



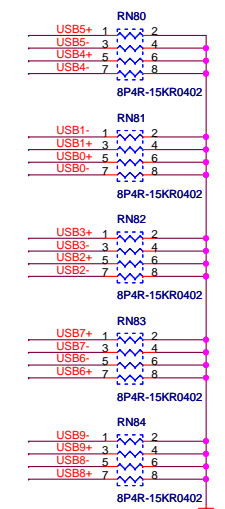
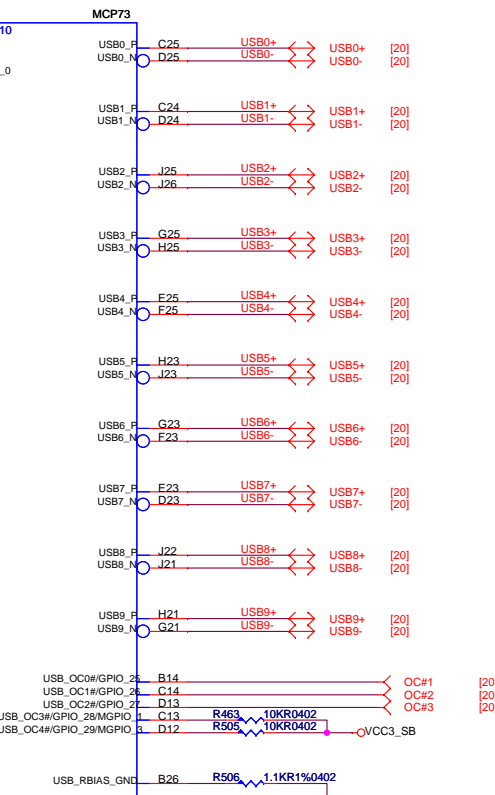
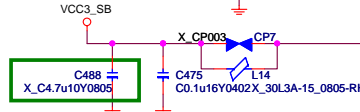
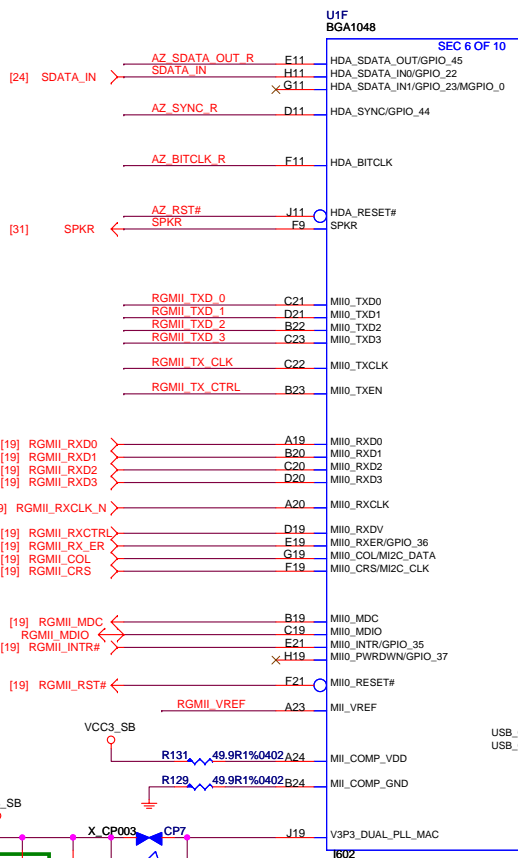
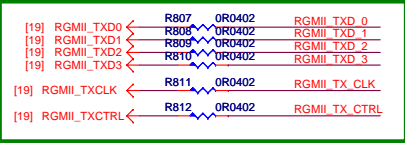


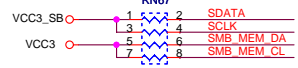
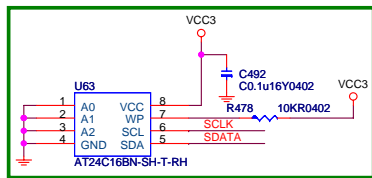


Strapping 10K ohm to VCC3_SB: RGMII

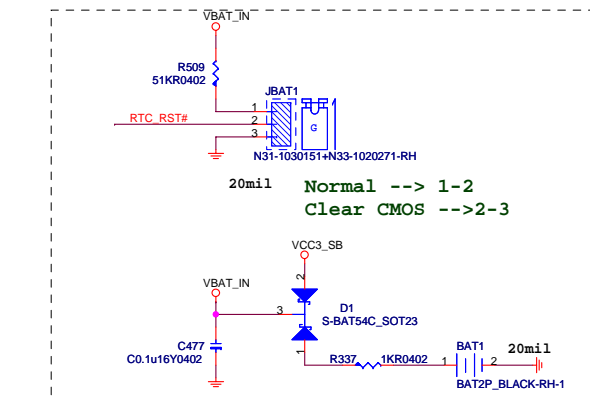
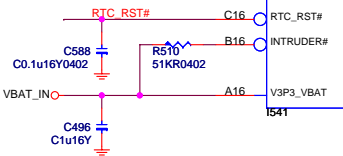
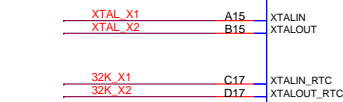
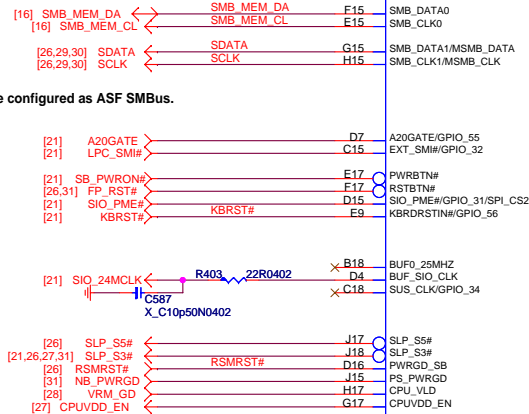
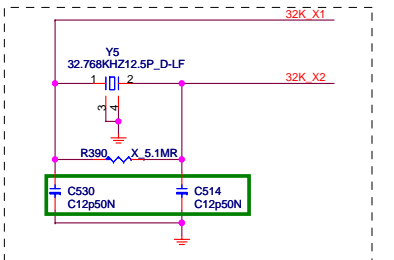
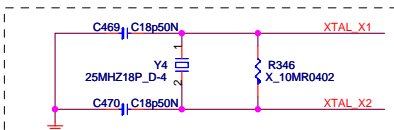
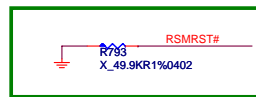
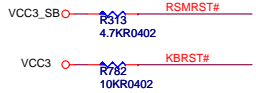


Close to U1

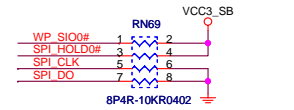
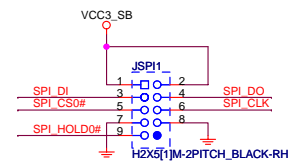
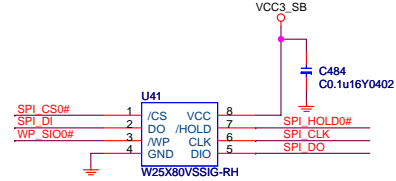
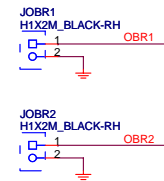
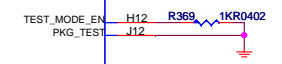
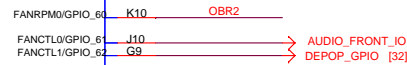
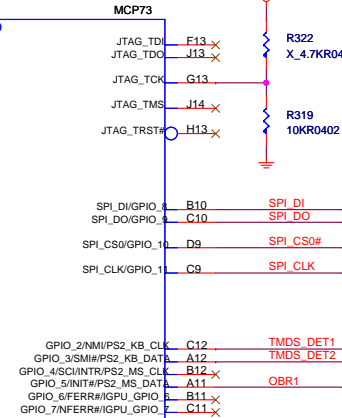




When SDATA/SCLK are not used, it can be configured as ASF SMBus.

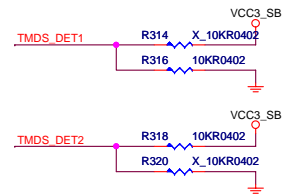


Normal --> 1-2
Clear CMOS --> 2-3



MCP73 SPI CLK STRAP

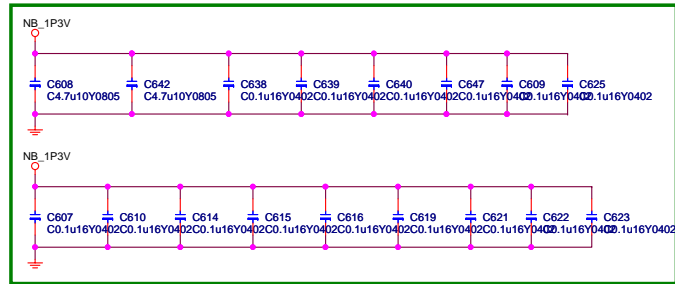
STRAP	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1



HDMI/DVI Detect

	TMD5_DET1	TMD5_DET2
DVI	1	0
HDMI	0	1
N/A	0	0

Bottom side



NB_1P3V	U11 BGA1048
AA12	V1P2_VDD_CORE
AA13	V1P2_VDD_CORE
AA19	V1P2_VDD_CORE
AA21	V1P2_VDD_CORE
AA22	V1P2_VDD_CORE
AA23	V1P2_VDD_CORE
AA24	V1P2_VDD_CORE
AA26	V1P2_VDD_CORE
AB12	V1P2_VDD_CORE
AB13	V1P2_VDD_CORE
AB15	V1P2_VDD_CORE
AB16	V1P2_VDD_CORE
AB17	V1P2_VDD_CORE
AB19	V1P2_VDD_CORE
AB21	V1P2_VDD_CORE
AB26	V1P2_VDD_CORE
AC12	V1P2_VDD_CORE
AC13	V1P2_VDD_CORE
AC17	V1P2_VDD_CORE
AC19	V1P2_VDD_CORE
AC21	V1P2_VDD_CORE
AC23	V1P2_VDD_CORE
AC24	V1P2_VDD_CORE
AC26	V1P2_VDD_CORE
AD12	V1P2_VDD_CORE
AD13	V1P2_VDD_CORE
AD17	V1P2_VDD_CORE
AD19	V1P2_VDD_CORE
AD21	V1P2_VDD_CORE
AD23	V1P2_VDD_CORE
AD26	V1P2_VDD_CORE
AE12	V1P2_VDD_CORE
AE26	V1P2_VDD_CORE
AH8	V1P2_VDD_CORE
AH9	V1P2_VDD_CORE
AJ10	V1P2_VDD_CORE
AJ6	V1P2_VDD_CORE
AJ8	V1P2_VDD_CORE
AJ9	V1P2_VDD_CORE
AK10	V1P2_VDD_CORE
AK6	V1P2_VDD_CORE
AK7	V1P2_VDD_CORE
AK8	V1P2_VDD_CORE
AK9	V1P2_VDD_CORE
AL6	V1P2_VDD_CORE
AL8	V1P2_VDD_CORE
AM4	V1P2_VDD_CORE
AM5	V1P2_VDD_CORE
AM6	V1P2_VDD_CORE
AN2	V1P2_VDD_CORE
AN3	V1P2_VDD_CORE
AN4	V1P2_VDD_CORE
AP3	V1P2_VDD_CORE
AP4	V1P2_VDD_CORE
AR1	V1P2_VDD_CORE
AR2	V1P2_VDD_CORE
AR3	V1P2_VDD_CORE
M23	V1P2_VDD_CORE
M24	V1P2_VDD_CORE
M25	V1P2_VDD_CORE
N23	V1P2_VDD_CORE
N24	V1P2_VDD_CORE
N25	V1P2_VDD_CORE
N26	V1P2_VDD_CORE
P26	V1P2_VDD_CORE
R18	V1P2_VDD_CORE
R20	V1P2_VDD_CORE
R22	V1P2_VDD_CORE
R24	V1P2_VDD_CORE
R26	V1P2_VDD_CORE
T18	V1P2_VDD_CORE
T20	V1P2_VDD_CORE
T22	V1P2_VDD_CORE
T26	V1P2_VDD_CORE
U18	V1P2_VDD_CORE
U20	V1P2_VDD_CORE
U22	V1P2_VDD_CORE
U23	V1P2_VDD_CORE
U24	V1P2_VDD_CORE
U26	V1P2_VDD_CORE
V15	V1P2_VDD_CORE
V16	V1P2_VDD_CORE
V17	V1P2_VDD_CORE
V18	V1P2_VDD_CORE
V20	V1P2_VDD_CORE
V26	V1P2_VDD_CORE
W20	V1P2_VDD_CORE
W21	V1P2_VDD_CORE
W22	V1P2_VDD_CORE
W23	V1P2_VDD_CORE
W24	V1P2_VDD_CORE
W26	V1P2_VDD_CORE
Y12	V1P2_VDD_CORE
Y13	V1P2_VDD_CORE
Y15	V1P2_VDD_CORE
Y16	V1P2_VDD_CORE
Y17	V1P2_VDD_CORE
Y18	V1P2_VDD_CORE
Y19	V1P2_VDD_CORE
Y26	V1P2_VDD_CORE

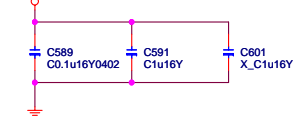
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SEC 8 OF 10

MCP73	V_FSB_VTT
V1P2_CPU_VTT	A31
V1P2_CPU_VTT	A32
V1P2_CPU_VTT	AB27
V1P2_CPU_VTT	AD27
V1P2_CPU_VTT	B31
V1P2_CPU_VTT	B32
V1P2_CPU_VTT	C31
V1P2_CPU_VTT	C32
V1P2_CPU_VTT	C33
V1P2_CPU_VTT	D31
V1P2_CPU_VTT	D32
V1P2_CPU_VTT	D33
V1P2_CPU_VTT	E31
V1P2_CPU_VTT	F29
V1P2_CPU_VTT	F30
V1P2_CPU_VTT	F31
V1P2_CPU_VTT	G29
V1P2_CPU_VTT	H27
V1P2_CPU_VTT	H28
V1P2_CPU_VTT	H29
V1P2_CPU_VTT	J27
V1P2_CPU_VTT	J28
V1P2_CPU_VTT	J29
V1P2_CPU_VTT	K29
V1P2_CPU_VTT	M27
V1P2_CPU_VTT	N27
V1P2_CPU_VTT	P27
V1P2_CPU_VTT	T27
V1P2_CPU_VTT	V27
V1P2_CPU_VTT	Y27

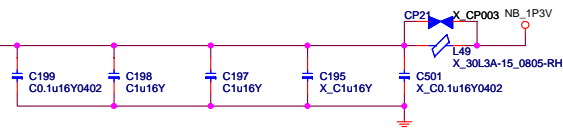
V_FSB_VTT

V_FSB_VTT

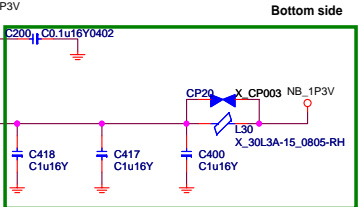


NB_1P3V	V1P2_PEX_DVDD
N13	V1P2_PEX_DVDD
R15	V1P2_PEX_DVDD
R16	V1P2_PEX_DVDD
T15	V1P2_PEX_DVDD
T16	V1P2_PEX_DVDD

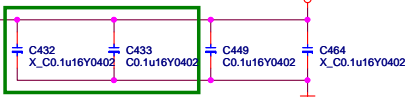
V1P2_PEX_AVDD	N12
V1P2_PEX_AVDD	P12
V1P2_PEX_AVDD	P13
V1P2_PEX_AVDD	T12
V1P2_PEX_AVDD	T13
V1P2_PEX_AVDD	U12
V1P2_PEX_AVDD	U13
V1P2_PEX_AVDD	W12
V1P2_PEX_AVDD	W13



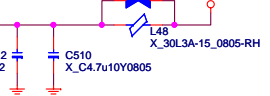
NB_1P3V	V1P2_SATA_DVDD
AD15	V1P2_SATA_DVDD
AE15	V1P2_SATA_DVDD
AE16	V1P2_SATA_DVDD
AG16	V1P2_SATA_DVDD




V3P3	AC6
V3P3	AC8
V3P3	AC9
V3P3	AG6
V3P3	AG8
V3P3	W6
V3P3	W8
V3P3	W9

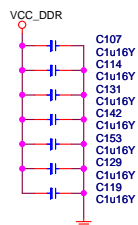
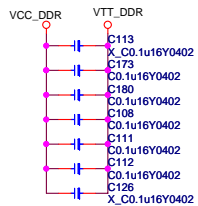
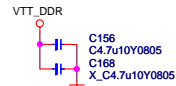
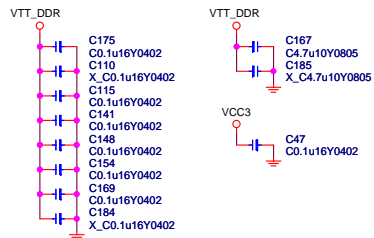


V3P3_DAC	F28
C512	F28
C510	F28

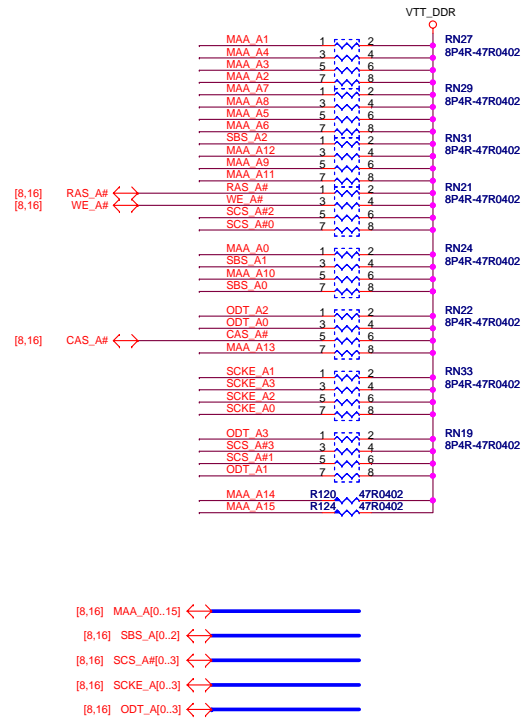


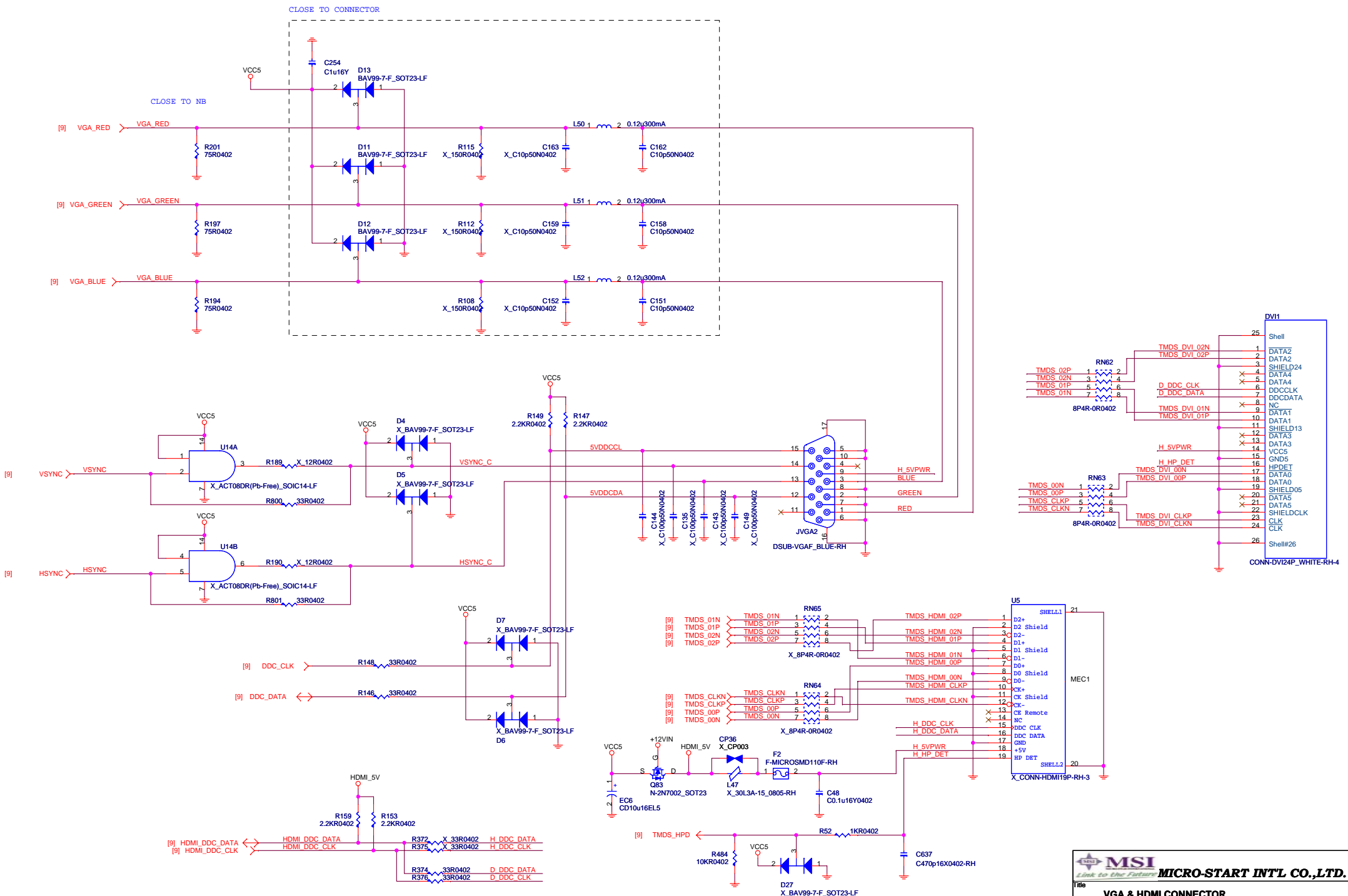
 MICRO-START INT'L CO.,LTD.		
Title		
MCP73 CORE/VTI POWER		
Size	Document Number	Rev
Custom	acer Persian / MS-7399	0A
Date:	Tuesday, August 07, 2007	Sheet 14 of 36

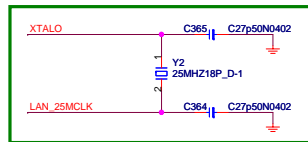
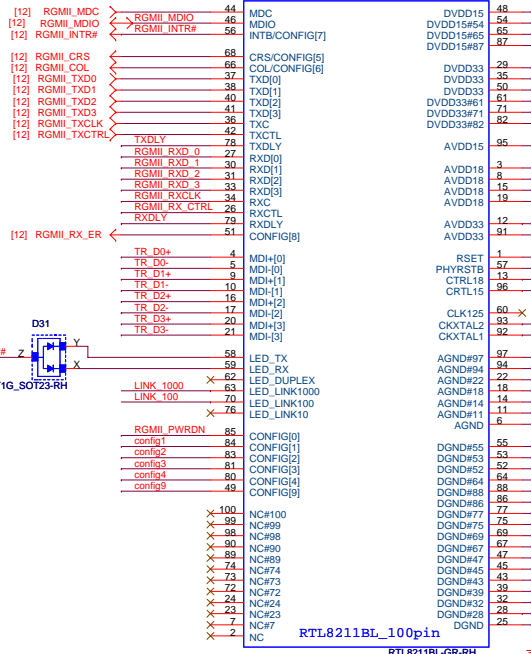
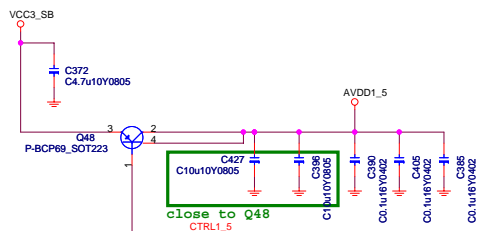
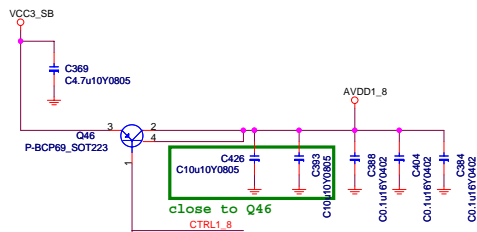
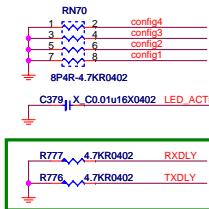
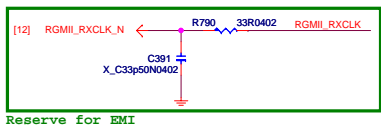
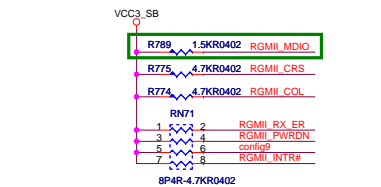
CHANNEL A VTT_DDR
DECOUPLING CAPS



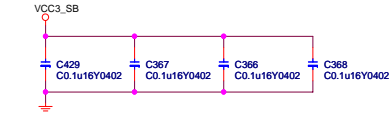
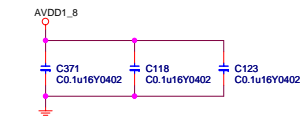
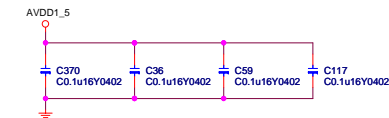
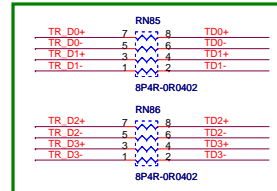
DDR II TERMINATION



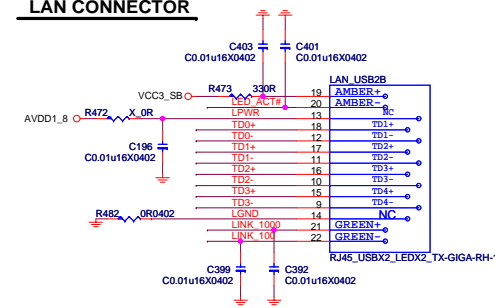




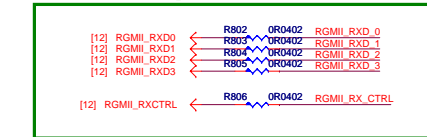
For EMI



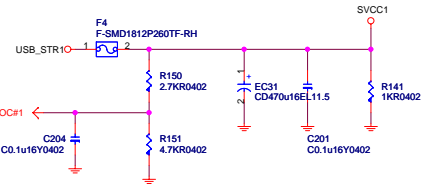
LAN CONNECTOR



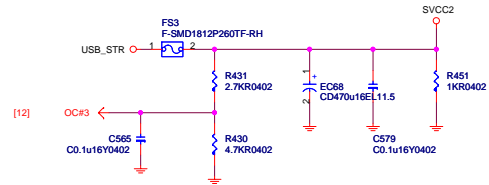
Close to LAN_Chip



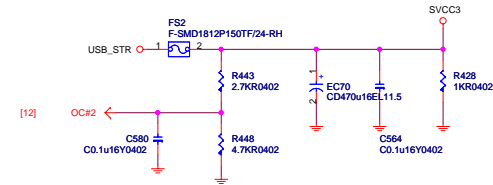
POWER CIRCUIT FOR USB PORT 0,1,2,3



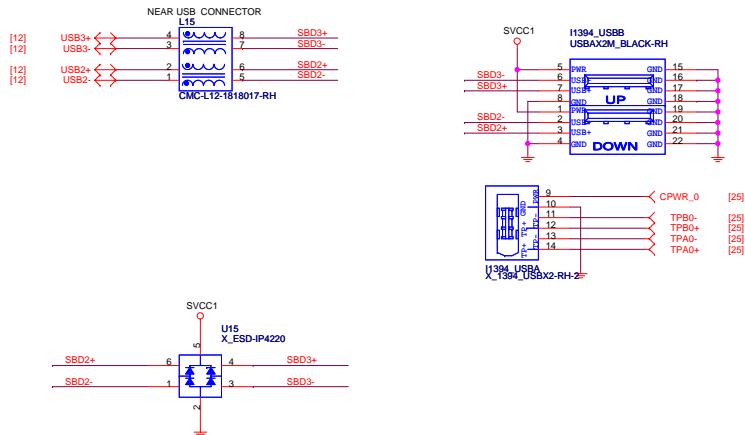
POWER CIRCUIT FOR USB PORT 4,5,6,7



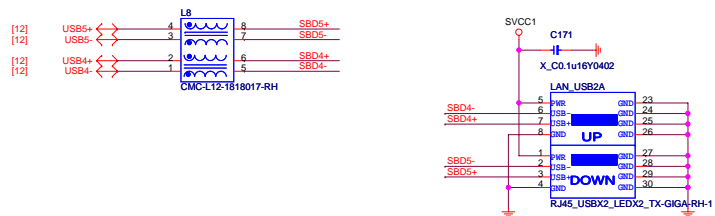
POWER CIRCUIT FOR USB PORT 8,9



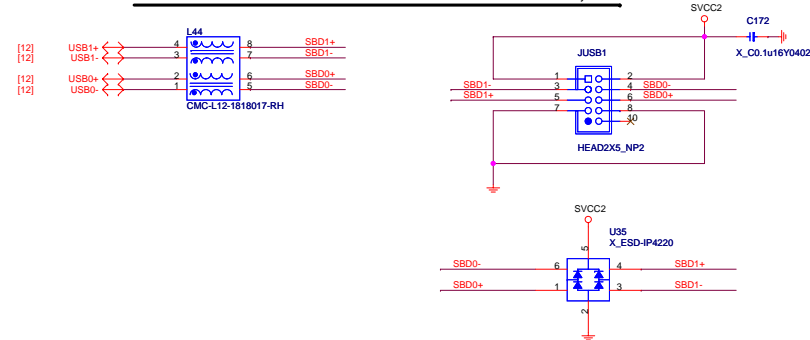
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



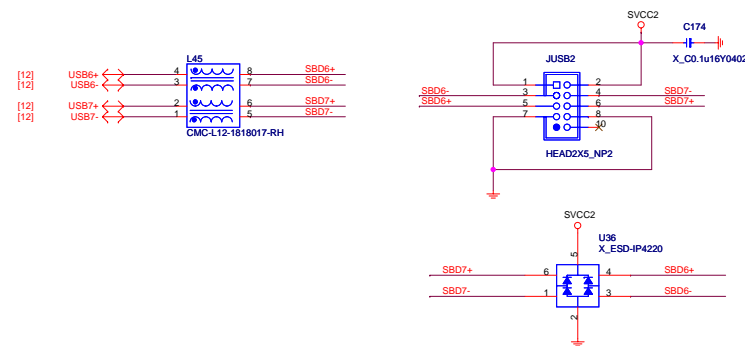
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



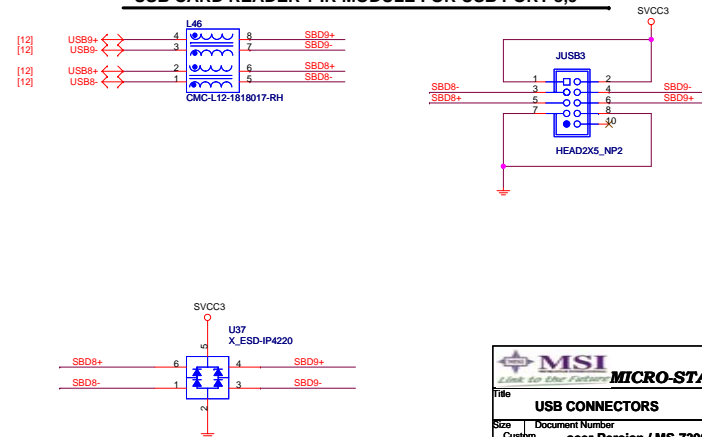
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5

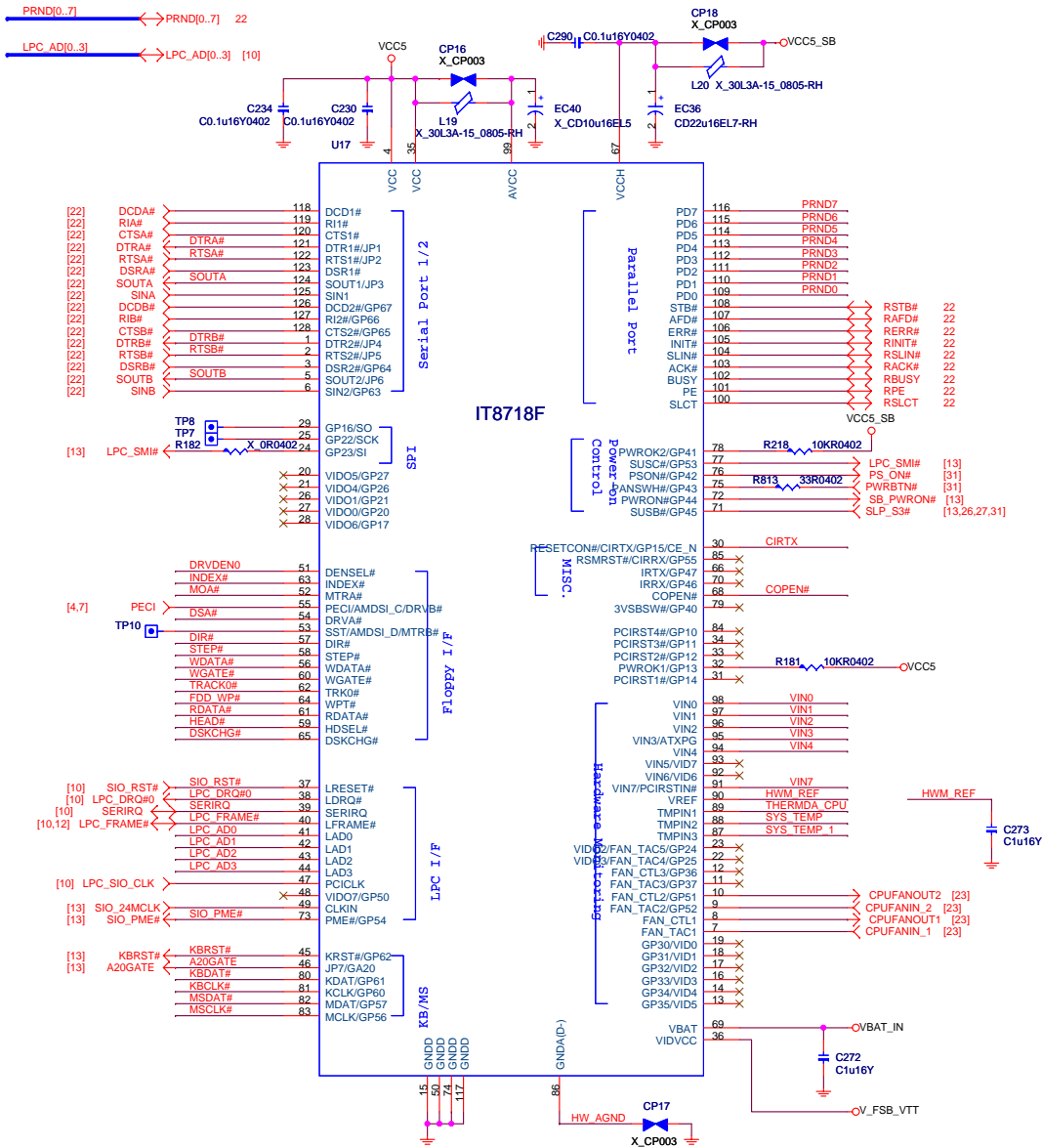


FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

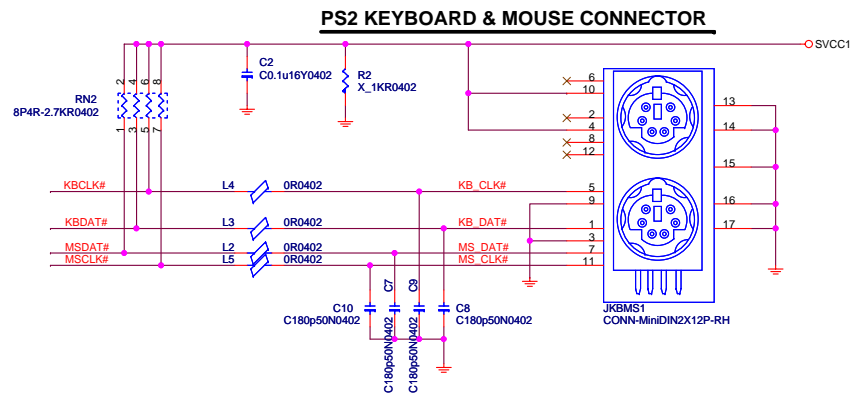


USB CARD READER + IR MODULE FOR USB PORT 8,9

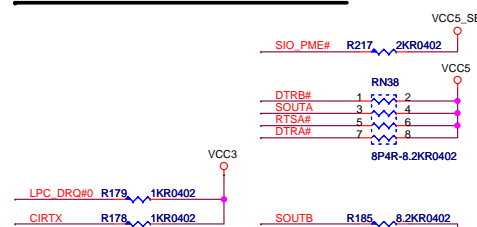




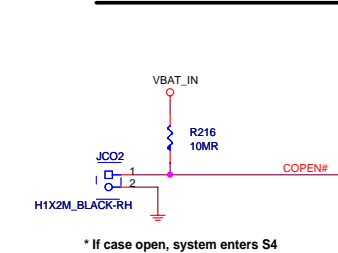
RTSB#	A20GATE	FAN DUTY
1	1	100%
1	0	75%
0	1	50%
0	0	25%



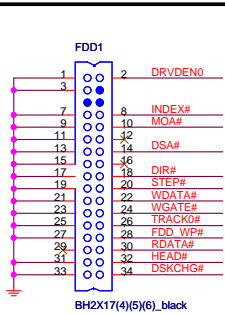
SUPER I/O STRAPPING RESISTOR



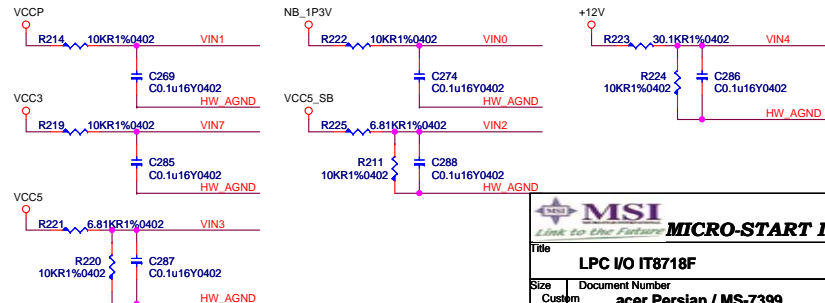
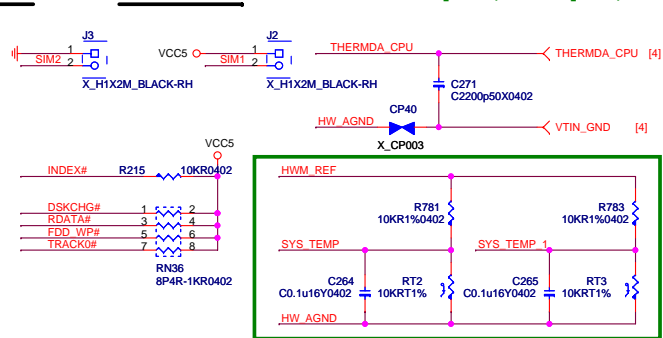
Chassis Intrusion



FLOPPY CONNECTOR

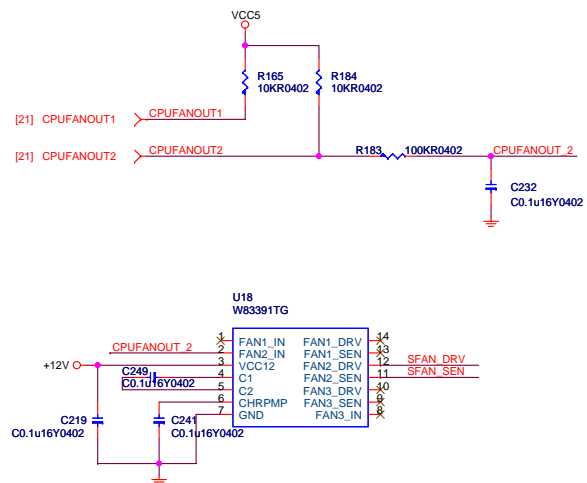


Simulation

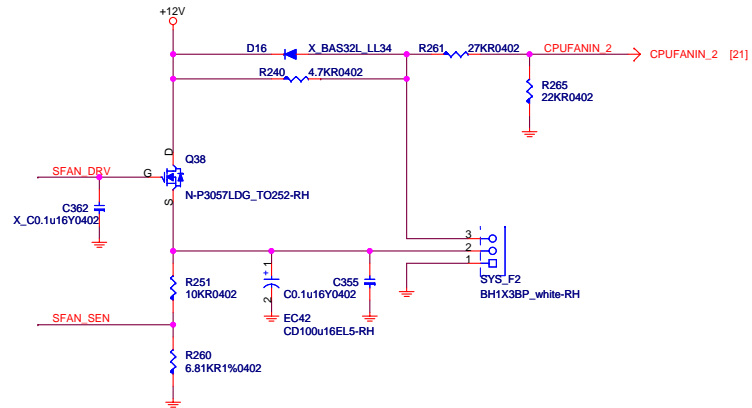


Title LPC IO IT8718F		
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Date: Thursday, August 23, 2007	Sheet 21	of 36

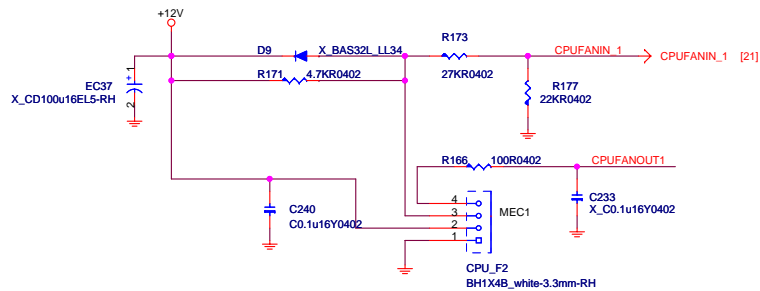
PWM FAN CONTROL



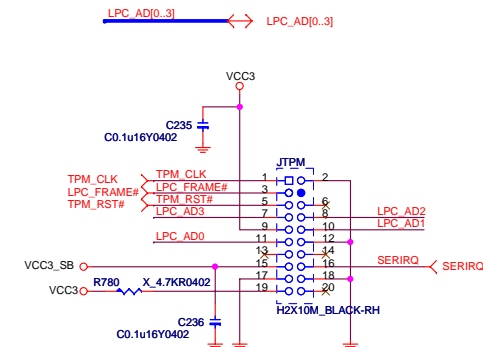
SYS FAN



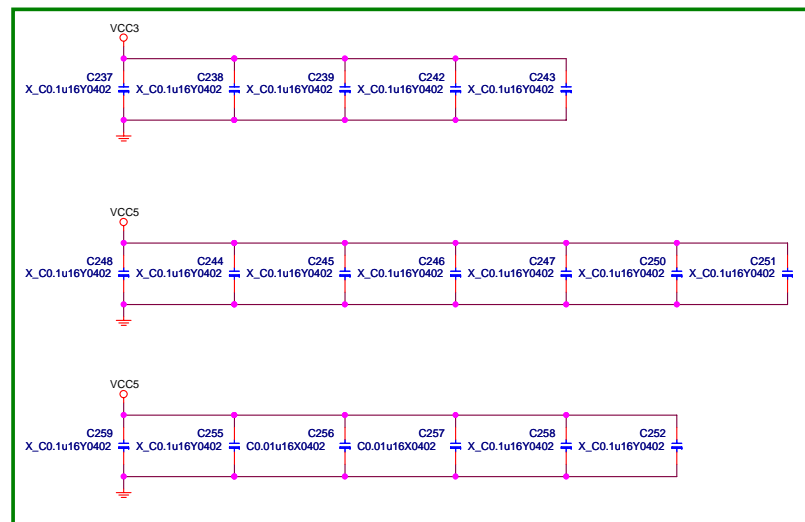
CPU FAN

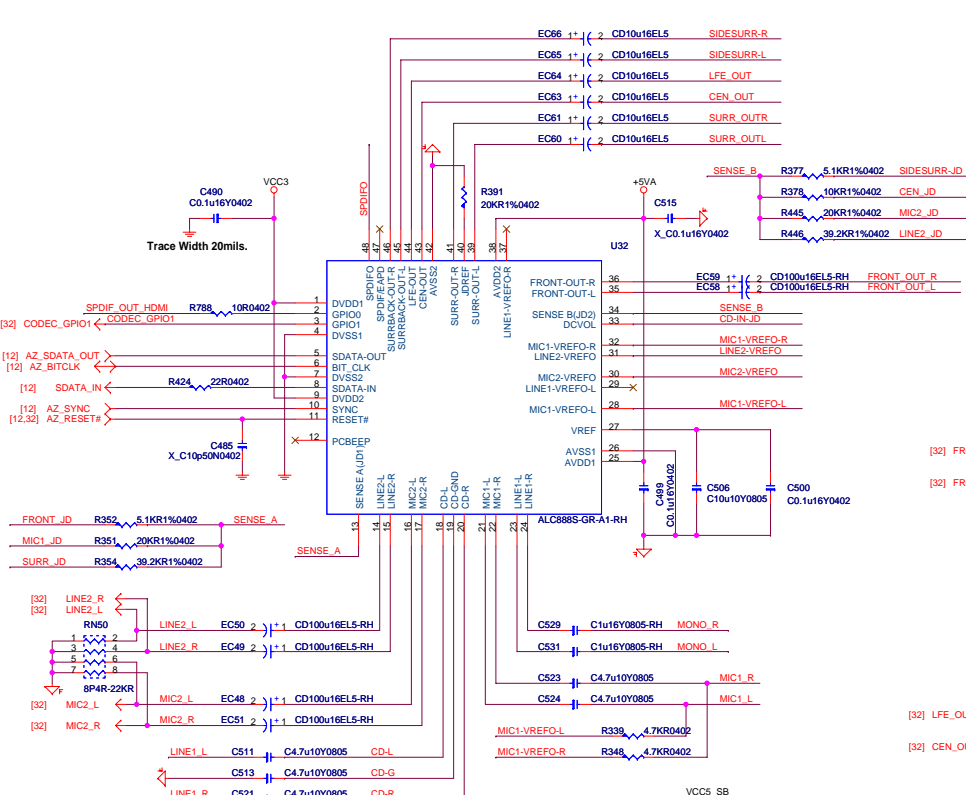


TPM Header

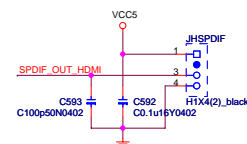


For EMI

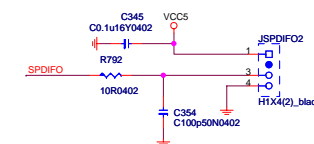




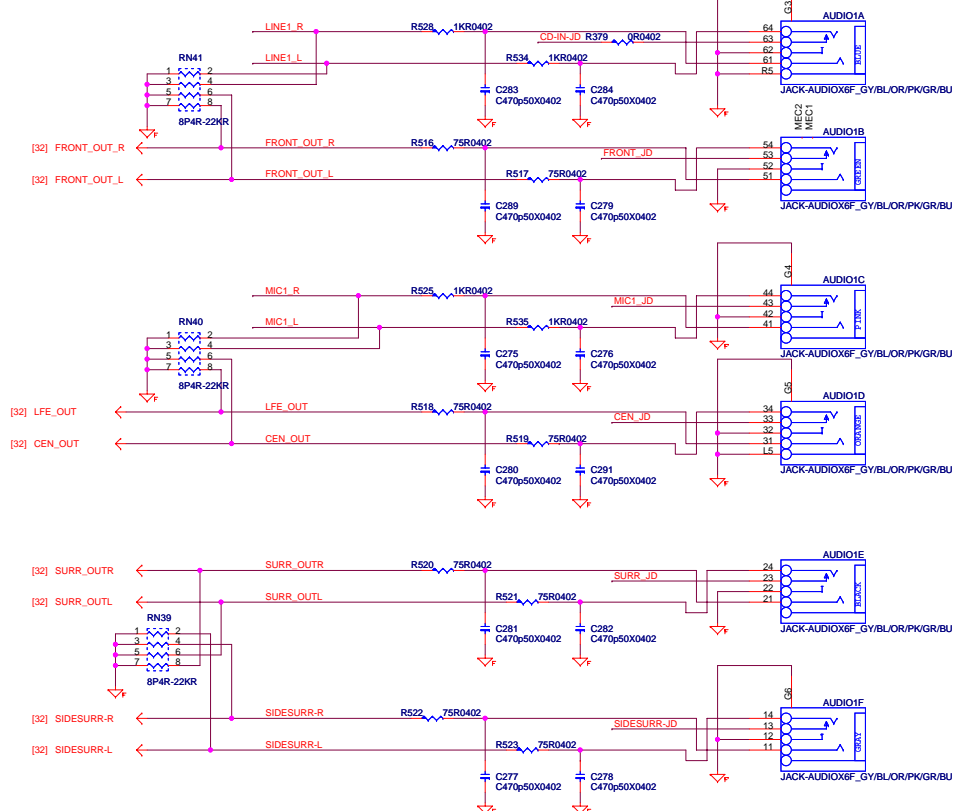
HDMI SPDIF HEADER



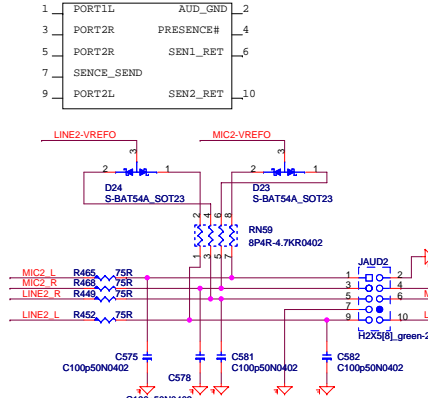
SPDIF HEADER



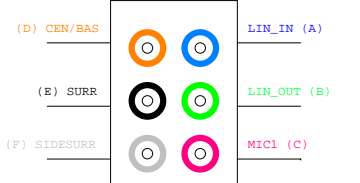
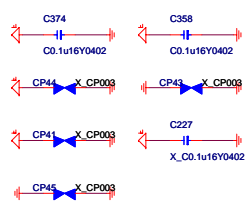
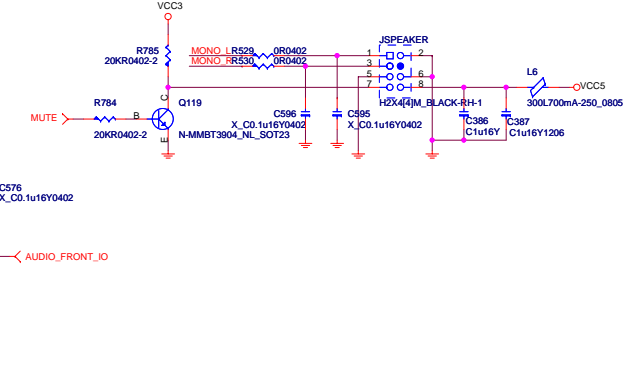
Rear audio jack



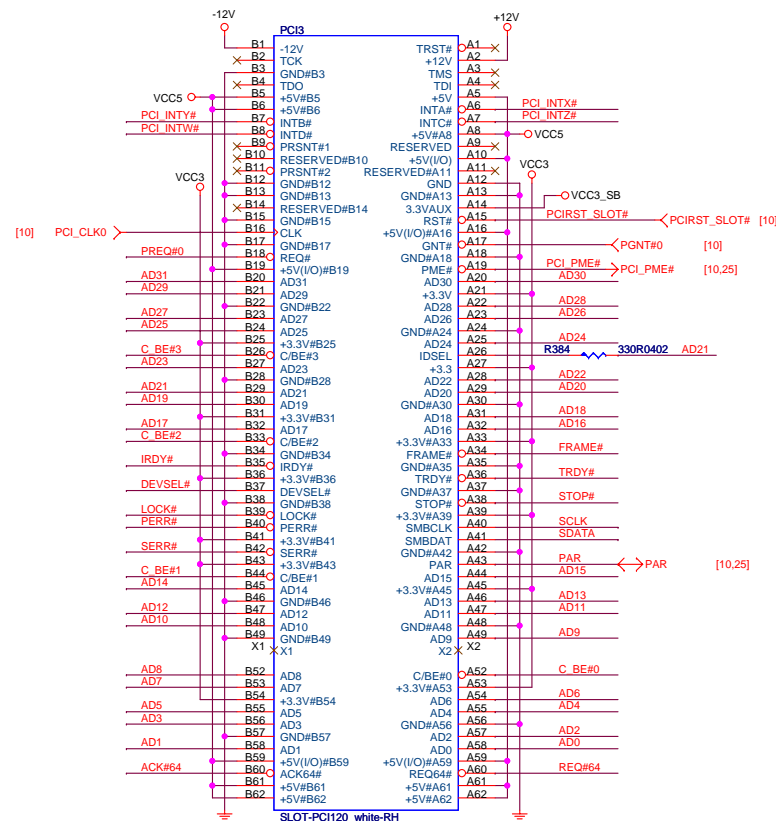
FRONT AUDIO PIN HEADER FOR AZALIA



Internal Speaker



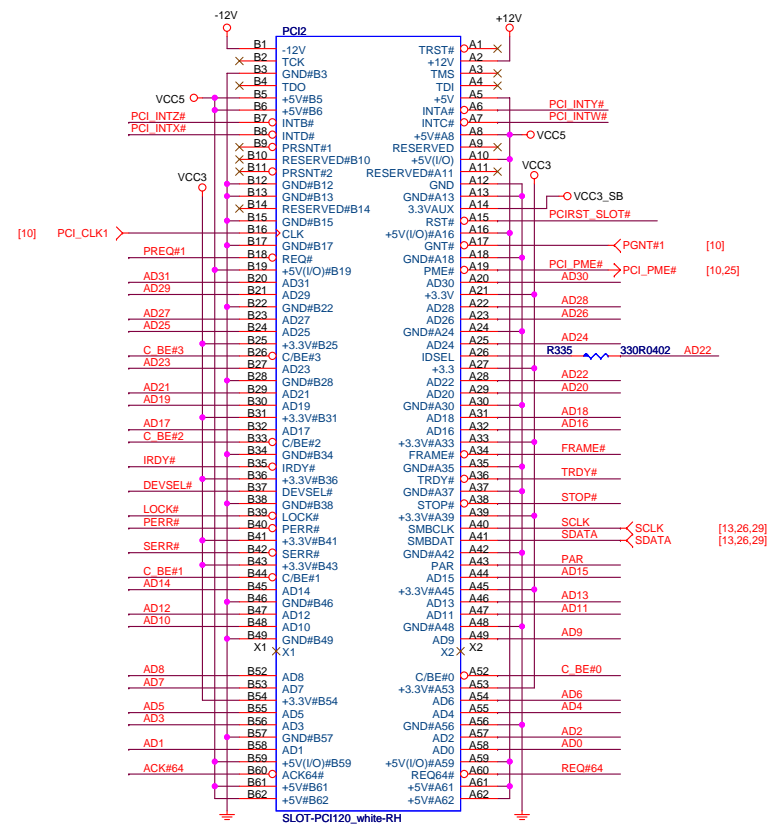
PCI SLOT 1 (PCI VER: 2.3 COMPLY)



IDSEL = AD21
MASTER = PREQ#0
PCI_INTX#

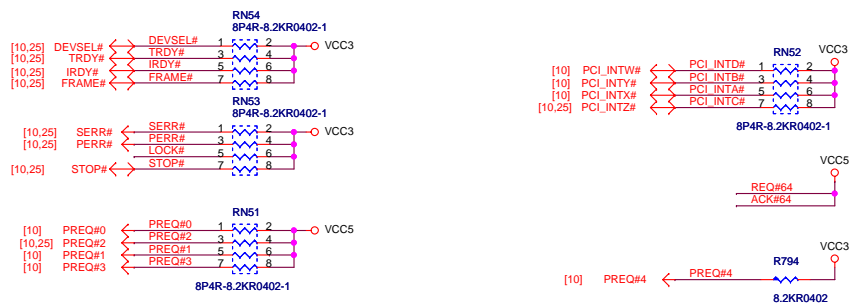
[10,25] AD[0..31] ← AD[0..31]
 [10,25] C_BE[0..3] ← C_BE[0..3]

PCI SLOT 2 (PCI VER: 2.3 COMPLY)

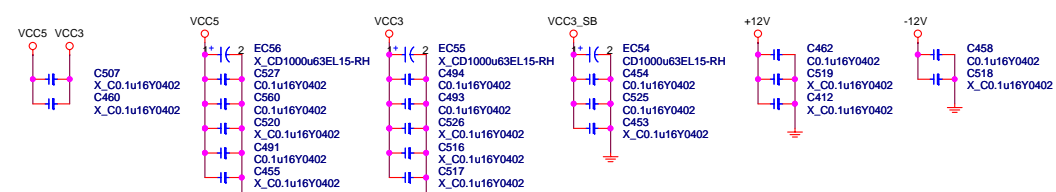


IDSEL = AD22
MASTER = PREQ#1
PCI_INTY#

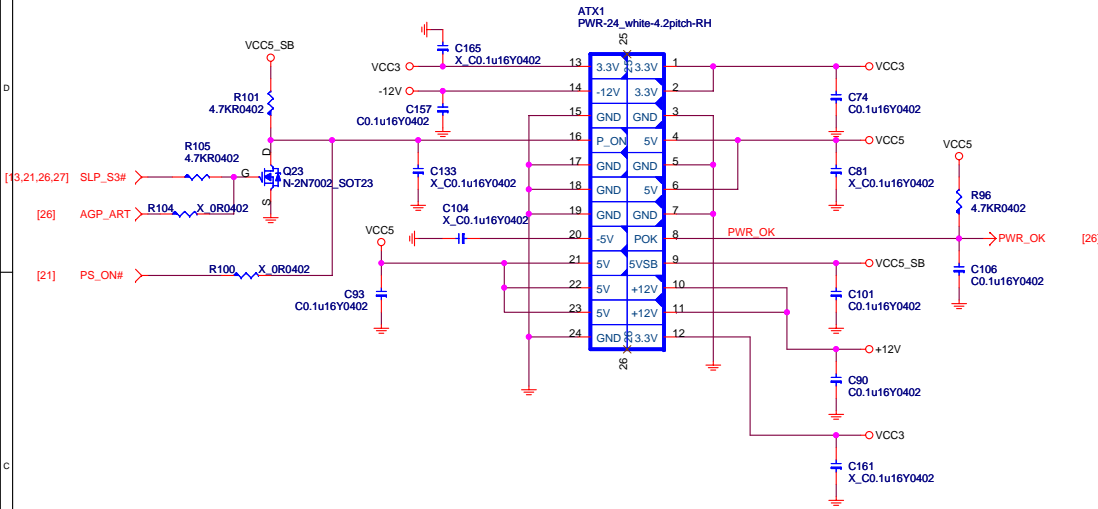
PCI PULL-UP / DOWN RESISTORS



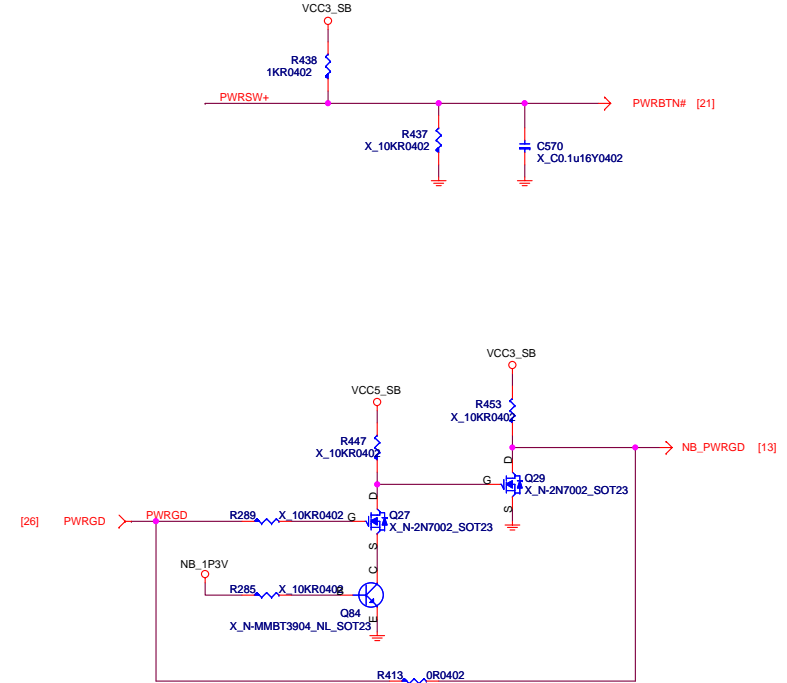
PCI SLOT DECOUPLING CAPACITORS



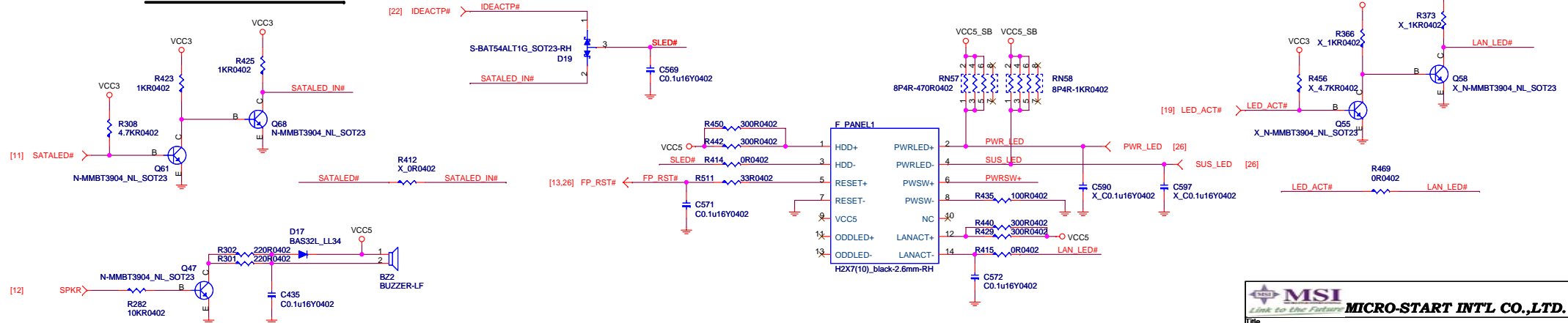
ATX CONNECTOR



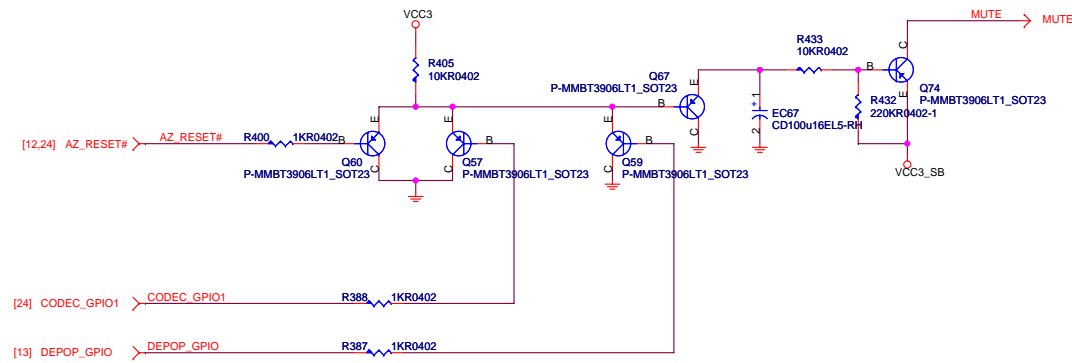
POWER BUTTON



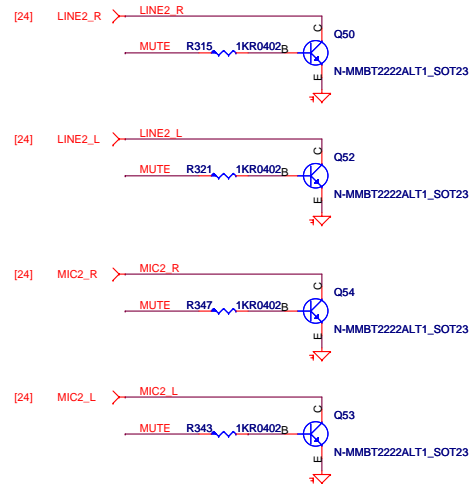
acer Front Panel Connector



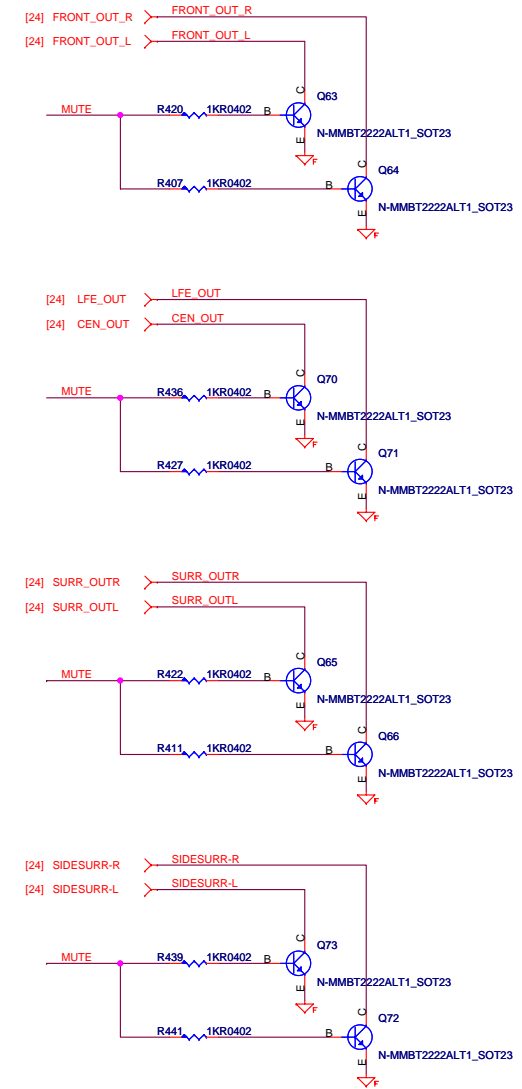
Audio De-Pop Control Circuit



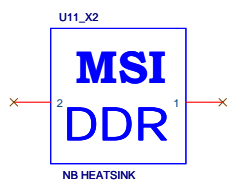
Front Audio Port De-Pop Circuit



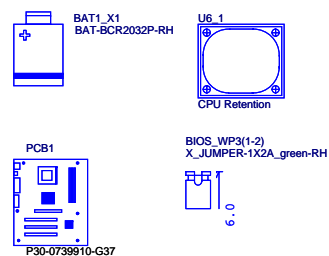
Rear Audio Port De-Pop Circuit



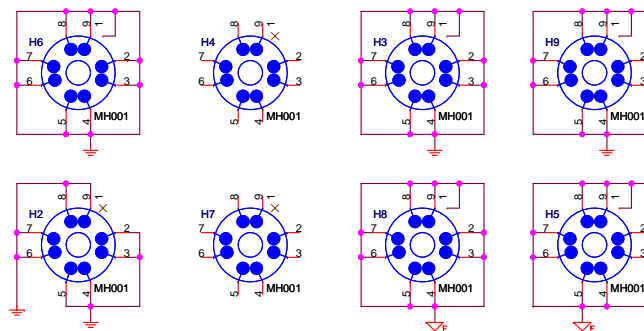
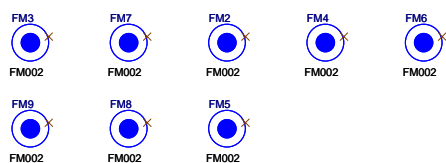
HEAT SINK

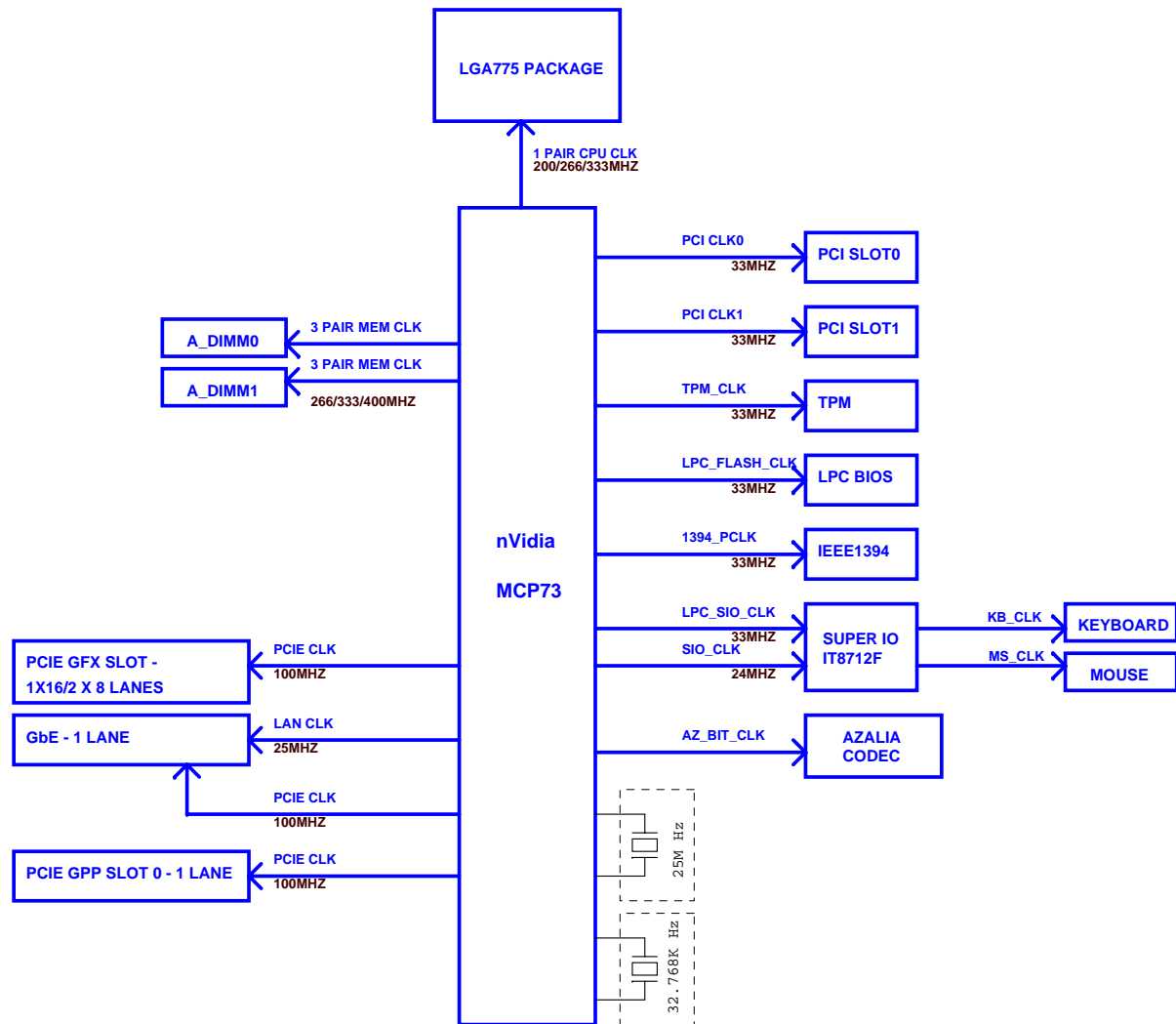


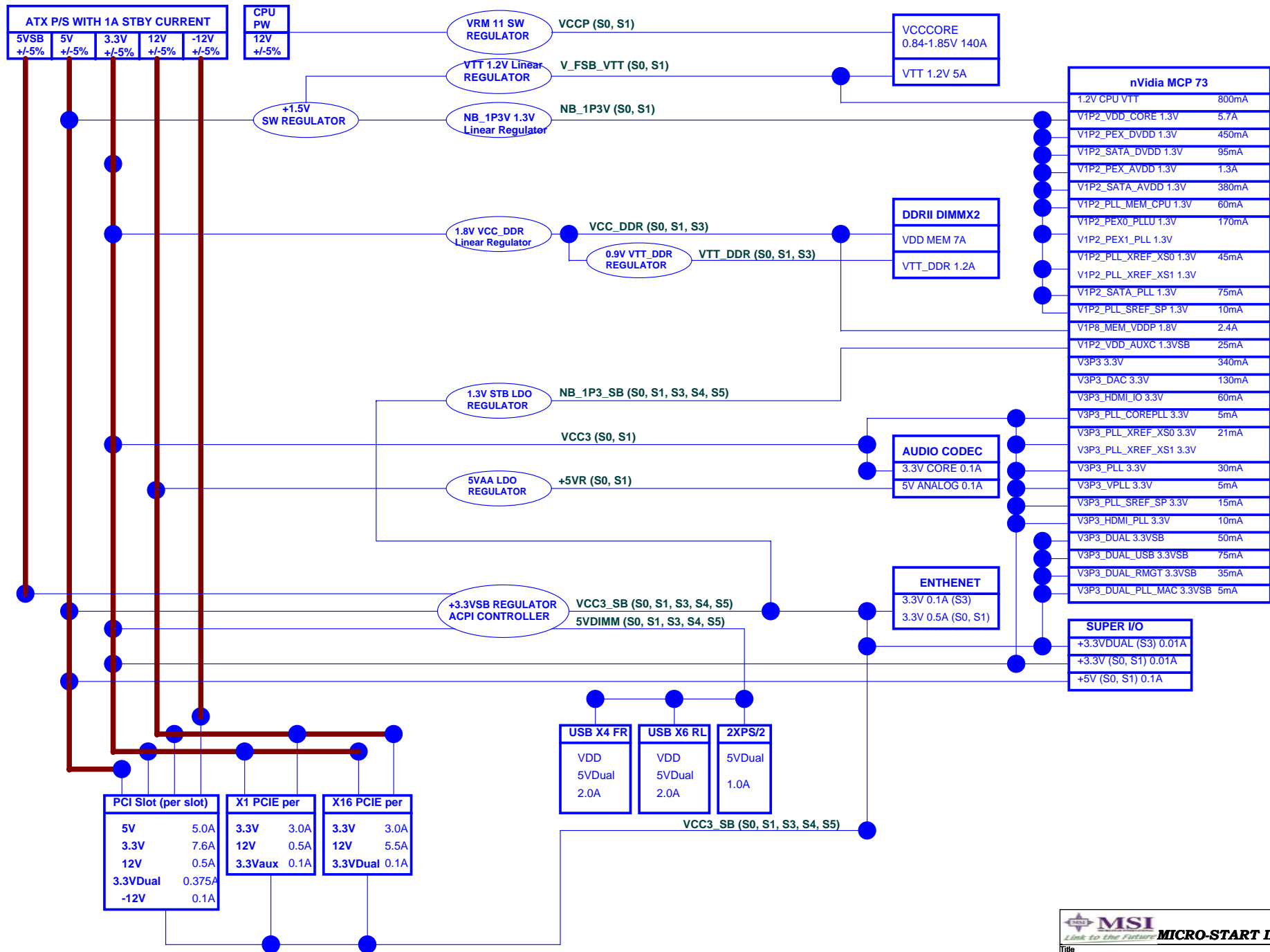
MANUAL PART

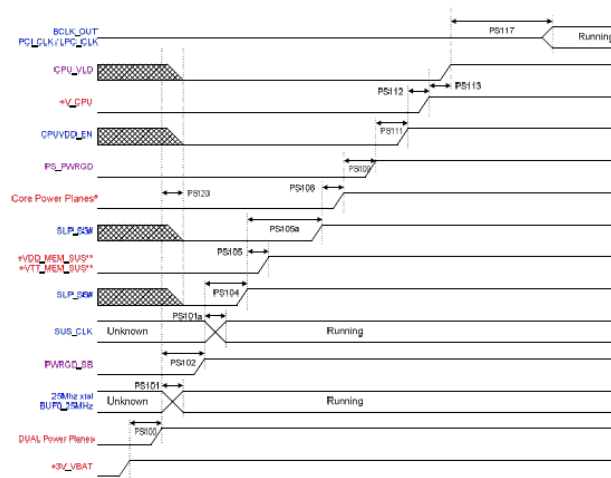


Optics Orientation Holes







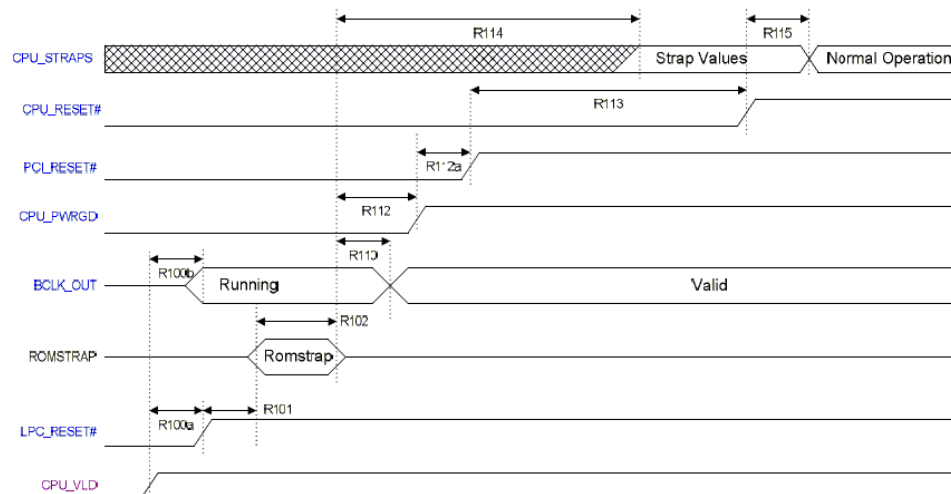


Power Planes in Red MCP73 output signals in Blue Motherboard generated signals in Purple

* Core Planes include:
All power planes without _DUAL or _SUS in the name except:
CPU Core Power Plane

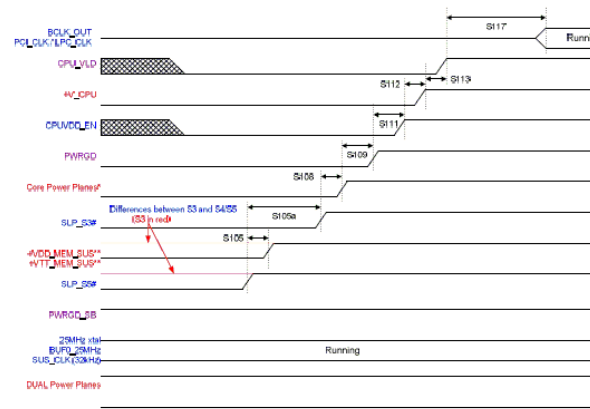
** DDR2 Memory Power Planes:
VDD = 1.8V
VTT = 0.9V

MCP73 G3-to-S0 Power-Up Sequence



MCP73 output signals in Blue Motherboard generated signals in Purple

MCP73 Cold Reset Power-Up Sequence

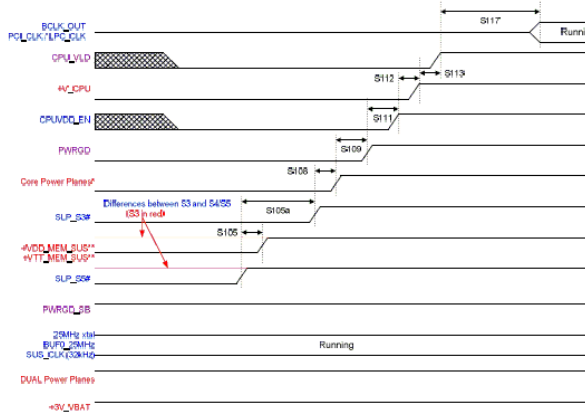


Power Planes in Red MCP73 output signals in Blue Motherboard generated signals in Purple

* Core Planes include:
All power planes without _DUAL or _SUS in the name except:
- CPU Core Power Plane

** DDR2 Memory Power Planes:
VDD = 1.8V
VTT = 0.9V

MCP73 S3/S4/S5 to S0 Power Resume Sequence



Power Planes in Red MCP73 output signals in Blue Motherboard generated signals in Purple

* Core Planes include:
All power planes without _DUAL or _SUS in the name except:
- CPU Core Power Plane

** DDR2 Memory Power Planes:
VDD = 1.8V
VTT = 0.9V

MCP73 S3/S4/S5 to S0 Power Resume Sequence